Built-In Test for Performance Characterization and Calibration of Phase-Locked Loops

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Built-In Test for Performance Characterization and Calibration of Phase-Locked Loops

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LIST OF ABBREVIATIONS

3G	3rd generation; 3rd generation of mobile telecommunications technology
4G	4th generation; 4th generation of mobile telecommunications technology
ADC	analog-to-digital converter
AFC	auto frequency calibration
BB	baseband
BER	bit error rate
BiCMOS	Bipolar CMOS technology
BIST	built-in self-test
CML	current mode logic
CMOS	complementary metal-oxide semiconductor
CP	charge pump
CUT	circuit under test
DUT	die under test
DAC	digital-to-analog converter
DSM	delta-sigma modulation
DSP	digital signal processing
FF	fast-fast (process corners)
FOM	figure of merit
FTR	frequency tuning range
g_m	transconductance
HDMI	high-definition multimedia interface
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IIP3	input-referred third-order-intercept point
IO	input output (interface)
IPTAT	current proportional to absolute temperature
IQ	in-phase and quadrature
K_{VCO}	gain of VCO
LC	inductor-capacitor
LDO	low drop-out regulator
LF	loop filter
LNA	low-noise amplifier
LO	local oscillator
LTE	long term evolution; a standard in 4G communication
LVDS	low-voltage differential signaling
MARS	multivariate adaptive regression splines
MOSFET	metal-oxide-semiconductor field-effect transistor
mmW	millimeter-wave
NF	noise figure
NMOS	n-channel MOSFET
P_{1dB}	1-dB gain compression point
PA	power amplifier

PCB	printed circuit board
PFD	frequency phase detector
PLL	phase-locked loop
PMOS	p-channel MOSFET
PSRR	power supply rejection ratio
PVT	process voltage temperature
RF	radio frequency
RMS	root mean square
RTL	register-transfer level
RX	receiver
SerDes	serializer/deserializer
SiGe	Silicon-Germanium
SoC	system-on-chip
SOI	silicon on insulator
SPO	static phase offset
SS	slow-slow (process corners)
TSPC	true-single-phase-clocking
TT	typical-typical (process corners)
TX	transmitter
USB	universal serial bus
VCO	voltage-controlled oscillator
WiGig	wireless gigabit
WLAN	wireless local area network
WPAN	wireless personal area network
XO	crystal oscillator

SUMMARY

With the development of communication technology, people are able to use different frequency bands to transmit data through the cable or the air nowadays. From kilobit to multi-gigabit, the bandwidth is increased promptly to cover a lot of applications such as wireless 4G network and wireline high-definition multimedia interface (HDMI) interface. At the same time, the hardware robustness of data transmission becomes critical for reliability, especially for high speed and wide bandwidth standards which rely on more design and verification efforts. Frequency synthesizer (also called phase-locked loop or PLL) is one of the most important hardware generating different frequency and bandwidth carrier in communication systems. It is therefore significant to guarantee the specifications over process, voltage, and temperature (PVT) variations from the phase of design and verification. The design process involves the setup of frequency plan, loop dynamics, and building blocks. PLL verification requires measurement of loop parameters, output frequency variation, and noise performance. Spectrum analyzer and oscilloscope are required for the tests, which are complicated and time-consuming processes. Built-in-self-test (BIST) and self-calibration are efficient methodologies since the diagnosis and healing are utilized an on-chip to save hardware and time cost.

The objective of this dissertation is to propose analog testing methods and self-calibration circuits of frequency synthesizer from the perspective of circuit design. A robust design of PLL is necessary to overcome PVT variations, while the testing and calibration schemes are required to detect the performances variation and adjust the specification outliers respectively with a minimum overhead of area, power, and time

consumption. The results serve as a combination on-chip solution of BIST and self-calibration.

Design of PLL is first introduced with adaptable loop acquisition speed. The settling time of different loop gain can be adjusted to 2.3 μsec to against PVT variation by this technique. While a 3.5GHz baseband CMOS PLL for reference generation is designed with capacitance amplification for 90% less area of loop filter, a 24GHz radio-frequency (RF) CMOS frequency synthesizer is designed to demonstrate to cover a wide tuning range of 7.7 GHz with dual-core voltage-controlled oscillator (VCO). The PLLs fit the requirement of advanced millimeter-wave (mmW) wireless transceiver.

For testing methodology of frequency synthesizer, analog based verification techniques are investigated. An integrator is used for PLL loop parameters and reference spur estimation. The integrator can be used in PLL alternate test methodology for response extraction. Both simulation and hardware measurement validate the sensor-based testing on loop parameters. In addition, the correlation between static phase offset (SPO) and reference spur is further analyzed for reference spur prediction. A programmable BIST design is proposed for SPO estimation with a minimum resolution of 10psec. The correlation between integrator outputs and reference spur is verified in a PCB-based design including a PLL and an integrator as well. The difference of integrator output DC voltage shows linear correlation with the reference spur performance.

Lastly, a PLL with self-calibration circuits is implemented in CMOS 65nm technology to validate the function of reference spur suppression. With the built-in SPO detector, the minimum and maximum improvement of reference spur is 12dB and 22.9 dB respectively. The PLL has an area overhead of 12.1 % with same current consumption.

CHAPTER 1: INTRODUCTION

1.1 Motivation

Life of humans has been changed dramatically by communication technology in the last two decades. Both wireline and wireless communication are evolving with high throughput. USB 3.0 supports a data rate of up to 5 Gbps [1], HDMI uses a transmission rate of up to 10.2 Gbps [2], DisplayPort has a throughput of up to 21.6 Gbps [3], and Thunderbolt provides a transmission speed of up to 20 Gbps [4]. Advanced RF applications compatible with these existing wireline interfaces are also developed rapidly to make wireless HDMI feasible. Mobile communication from 3G to 4G LTE network is improved with data transmission above one gigabit per second. Wireless Local Area Network (WLAN) features mid-range high speed protocol with IEEE 802.11ad as a new generation standard which combines the Wireless Personal Area Network (WPAN) mmW multi-gigabit capability [5-8] with WLAN.

In all communication hardware, a frequency synthesizer plays the role of clock generation for a communication system such as transceiver frequency conversion, serial and de-serial interface, and clock distribution. Frequency synthesizer takes advantage of phase comparison and is also called a phase-locked loop (PLL). Its performance is important for data integrity and high throughput. Conventional tests for integrated circuits involve external equipment and automation. The overall process is costly and time-consuming. An efficient test methodology and self-calibration circuit can provide internal observation with adequate accuracy. As a result, self-calibration circuits are useful because of the low-cost test method.

BIST function is viable for efficient on-chip measurement without the limitation of external equipment setup [9-11]. Many system-on-chip designs explore the BIST techniques to scan the performance via digital and analog circuit implementation that greatly reduces the off-chip cost. The self-test information can serve as important feedback for simultaneous adaption or improved design. On the other hand, calibration strengthens the robustness of circuits and systems to against PVT variation. In 2001, the calibration of PLL frequency is proposed [12]. Automatic frequency calibration (AFC) is demonstrated in a closed-loop operation. The fact controlling voltage of PLL converges to a static voltage is used for frequency comparison.

Although the BIST and calibration techniques seem to be promising, actual application with frequency synthesizer has the concern of trade-off between accuracy and cost overhead. An robust BIST design may verify the performances with two times area or power overhead which may not be used in conventional operation. On the other hand, the implementation of PLL BIST requires precise timing control for noise capture. The requirement becomes more and more difficult as the frequency generation is higher and higher. For the calibration circuits, conventional techniques focus on either frequency correction or dedicated circuits for parameter optimization. A solution for detecting and calibrating the performance of loop dynamics and noise is preferable.

In this research, we try to achieve a balance between performance and additional cost on the test and calibration for on-chip fabrication. The purpose is to explore mixed-signal testing methods and self-calibration circuit of PLL for advanced communication systems with a minimum overhead on cost.

1.2 Challenges

Design, test, and calibration of frequency synthesizer are the core concept of this research. Each topic has technical challenge individually but is closely related to each other at the same time. While a robust design is the basis of solid circuit performances, an accurate test is necessary to validate the hardware function. Also, an effective calibration can even make the circuit design more robust with adequate feedback.

The design of PLL involves the consideration of stability, bandwidth, locking range, noise, area, and power consumption [13]. The area and power are especially important factors for low cost low power application, which is the case for wireless transceiver baseband and serializer/deserializer (SerDes) [14-15]. Power budget is assigned to front-end circuits and high-speed IO with essential requirement for signal integrity over PVT on the channel path directly. On the other hand, RF frequency synthesizer suffers PVT variation seriously in mmW application emerging for high throughput. The variation of frequency can be examined by the equation for VCO adopting cross-coupled inductor-capacitor (LC) tank structure [16]. The oscillation frequency can be expressed as

$$W_{osc} = \frac{1}{\sqrt{L \cdot C}}, \tag{1}$$

where L and C are the inductor and capacitor values in the tank. Assume the inductor value is kept the same the frequency variation can be derived from Equation (1) and expressed as

$$\frac{\partial W}{\partial C} = -\frac{W}{C}, \tag{2}$$

where ∂W is the oscillation frequency variation based on a capacitance variation ∂C. According to Pelgrom's Law, device mismatch is inversely proportional to the device area [17], which can be applied for a comparison between 2.4GHz WLAN and 60GHz WPAN application. If a 1% variation of capacitance occurs in a 2.4GHz VCO with an 2nH inductor and a 2.2pF capacitor, the resulted frequency mismatch is 24MHz. However, the passive components would be much smaller than those in WLAN application. Assume a 48GHz VCO is used for 60GHz super-heterodyne transceiver with a 400pH inductor and a capacitance 27fF in the same process and fabrication wafer, the device area for capacitor is about 81 times smaller than that in the 2.4GHz tank. As a result, the variation is 9% larger with 4.32GHz frequency shift. RF band coverage is actually a strict specification for 60GHz designers because the parasitic effect of manufacturing can easily change the value by few femto farad.

Test and design share the same challenging constraint in terms of strict specification. High frequency imposes high cost on testing equipment and process for subtle precision. Signature test has been used in RF and analog test such as power amplifiers, low-noise amplifier, and transceiver. A stimulus would be generated and injected the device under test (DUT) for specification evaluation [18-20]. The evaluation can be optimized by different sensors based on the output signature. However, this technique has never been applied to frequency synthesizer related circuits. It is of concern to generate an adequate trigger and detect the output values for specification evaluation.

People has investigated AFC by different circuit techniques from the perspective of time, area, and accuracy efficiency [21]. Noise is of interest for PLL but seldom verified via on chip calibration. Circuits techniques to reduce the noise impact from spur

and VCO itself are proposed in many publications for deterministic and random jitter. However, it is still formidable to implement a corresponding noise sensor for a complete loop operation of self-calibration. The effectiveness of calibration and self-healing in terms of minimum fabrication overhead is very significant. When the auxiliary circuits occupies resource as much as the main device, the additional cost is inefficient.

1.3 Organization

The content is organized as follows: chapter 1 starts with research objective and challenges followed by an overview of frequency synthesizer in chapter 2. Frequency synthesizer serves as backbone in this research. Conventional architectures and loop analysis are introduced with the role of PLL in applications as well as the frequency plan in mmW system. The specification, calibration, and relevant state-of-the-art techniques of PLL are then investigated.

Chapter 3 introduces the design of frequency synthesizer at transceiver baseband and RF. Performances are emphasized with minimum overhead against PVT variation. Fast settling of PLL is required for high-throughput system when a prompt switch between channel communication occurs. Settling time is determined by bandwidth which suffers from PVT corners for gain and analog performance change. Modification of bandwidth can vary acquisition time at the same time. However, the trade-off between settling time and phase margin may affect the loop stability. Bandwidth adaptability is therefore analyzed and designed in a 24GHz PLL to overcome the PVT variation on acquisition speed and trade-off.

In order to improve area efficiency in a loop filter, a capacitance amplifier is designed in a 3.5GHz PLL with compatible performance for baseband synthesizer. It

serves as not only the clock source for backend circuits but also a reference clock for IF and RF PLL. On the other hand, RF PLL has to cover a carrier bandwidth of 6.48 GHz for 60GHz application. A dual-core VCO design is used to solve the issue of frequency range affected by parasitic values of circuits. Chapter 3 provides solutions in PLL design to overcome adaptability, area efficiency, and frequency coverage issues. The summary of this dissertation can be shown in Figure 1.1, which includes critical test and calibration of PLL.

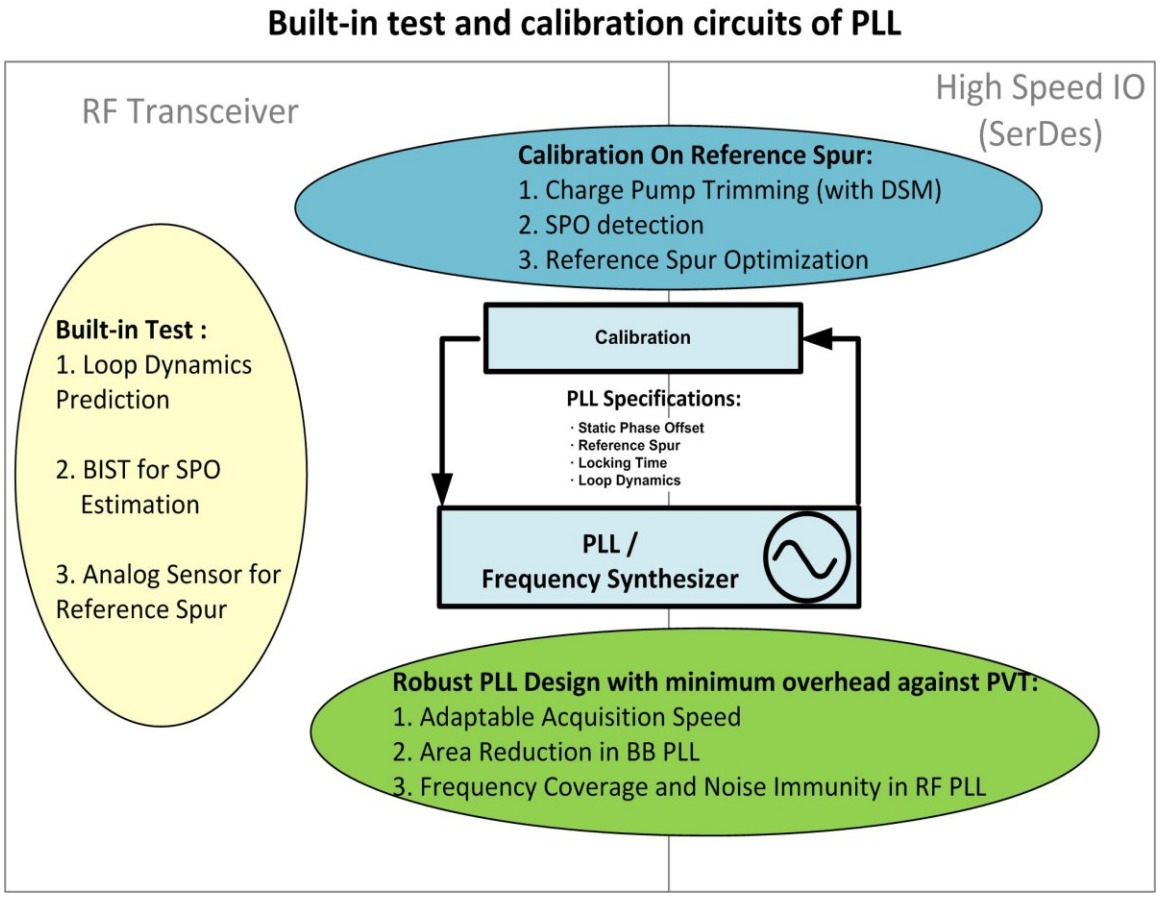


Figure 1.1. Summary, critical blocks, and challenges of PLL design, test, and calibration.

Chapter 4 introduces testing methodology based on analog signatures for frequency synthesizer specification verification. Different testing methodologies

including DSP technique and alternate test are introduced. An analog sensor is then developed and analyzed for PLL loop parameters and reference spur testing. For loop parameters, a 1-5GHz CMOS PLL is designed for analog features extraction from sensitive node. Analog sensors are applied for evaluating responses and mapping the specifications of DUT by supervised learning. Experimental results of response extraction are obtained and verified in a 7GHz RF PLL. A BIST design is then proposed for static phase offset (SPO) estimation based on the fact that analog sensors are capable of acquiring performance signature. SPO is closely related to reference spur in PLL and can serve as in indicator for long-term jitter. In order to validate the correlation between the sensor output and the reference spur, a PCB-based PLL with charge pump programmability and a sensor are designed, and show the linear correlation in measurement.

Self-calibration of frequency synthesizer including the tuning and detection circuits is introduced in chapter 5. A 65nm CMOS PLL is designed with charge pump current trimmer and SPO detector. The charge pump current trimmer adjusts the charge and discharge current ratio so that the output SPO achieves an optimal result which indicates an optimal reference spur performance. A minimum and maximum spu improvement of 12dB and 22.9dB are obtained in measurement for output frequency from 400 MHz to 1 GHz.

The contribution of this dissertation is summarized in chapter 6. Potential development and challenge are discussed for future work in the end.

CHAPTER 2: FREQUENCY SYNTHESIZER OVERVIEW

2.1 Introduction to Frequency Synthesizer Architecture

A frequency synthesizer is a negative feedback system, which locks the frequency of the output clock according to the input reference clock. A conventional structure of a frequency synthesizer is shown in Figure 2.1. The synthesizer is phase-locked because the feedback comparison is done for the phase in phase/frequency detector (PFD). Any phase difference would control the charge pump (CP) to output a current and indicate the correction direction of frequency. The charged node has to be filtered through the loop filter (LF) for stability. This filtered voltage will then be connected to voltage-controlled oscillator (VCO), which generates a signal whose frequency is varied linearly with the input voltage.

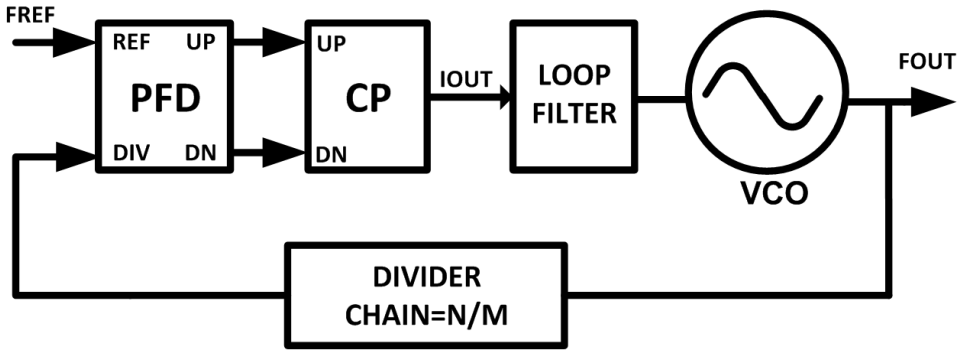


Figure 2.1. A conventional architecture of an integer/fractional phase-locked loop. N is equal to an integer, and M is equal to one when a integer mode is applied.

The feedback chain is composed of frequency dividers so that output signal can be multiple times of the reference clock. By updating the division ratio, different output frequencies can be synthesized for different channels. The division ratio can be expressed by N/M. For integer division, N is an integer number indicating the ratio between the

output frequency and the input frequency, and M is equal to one. When M is an integer, the synthesis is operated in fractional mode. The output can be stepped in a small ratio of reference frequency.

The loop can be analyzed by the open-loop transfer function with liner modes of each block shown in Figure 2.1. The open-loop transfer function can be expressed as

$$H_{ol}(s) = \frac{M \cdot K_{PFD} \cdot I_{CP} \cdot Z(s) \cdot K_{VCO}}{N \cdot 2\pi \cdot s}, \quad (3)$$

where K_{PFD} is the gain of PFD, I_{CP} is the current of CP, Z(s) is the impedance of LF, K_{VCO} is the gain of VCO (usually expressed in Hz/volt), and N/M is the division ratio. For a given loop bandwidth and phase margin, the specifications of each block can be derived from the Equation (3). Inversely, if parameters of each circuit are defined, the phase margin and loop bandwidth can be calculated.

2.2 Frequency Synthesizer in Communication Systems

Conventional transceiver architectures, including direct conversion and super heterodyne, are shown in Figure 2.2 PLL generates the required clock for carrier conversion. A direct conversion transceiver is a straightforward architecture to implement the wireless transceiver. One frequency conversion is utilized in the transmitter and receiver chain. In the example of 60GHz system, the PLL has to not only cover the 7GHz bandwidth but also support quadrature signals for RF IQ Mixers. The four used RF channels frequencies are 58.32 GHz, 60.48 GHz, 62.64 GHz, and 64.8 GHz. Direct conversion transceiver has the advantage of less power consumption and hardware cost than a super-heterodyne system. But it is also a challenge to cover the whole band on 60 GHz by one PLL [22].

On the other hand, the super-heterodyne transceiver as shown in Figure 2.2 has two frequency conversions in the transmitter and receiver. This system has two frequency interfaces. It uses 48 GHz as radio frequency (RF) and 12 GHz as intermediate frequency (IF) for 60GHz transceiver. The complexity of system is higher than direct conversion with two PLLs, two mixers, and IF circuits. A 7GHz bandwidth is still required for RF PLL, but the bandwidth centered at lower frequency (from 60 GHz to 48 GHz in this case), which provides more margin for circuit design. Also, the frequency of IF circuits is fixed. Some system plans adopt a sliding IF architecture with a fixed RF frequency, which is not practical. The sliding IF architecture requires a 7GHz bandwidth on the IF PLL, amplifiers, and mixers. It is inefficient to design such IF circuits with this wide bandwidth. A lot of power will be consumed [23-24].

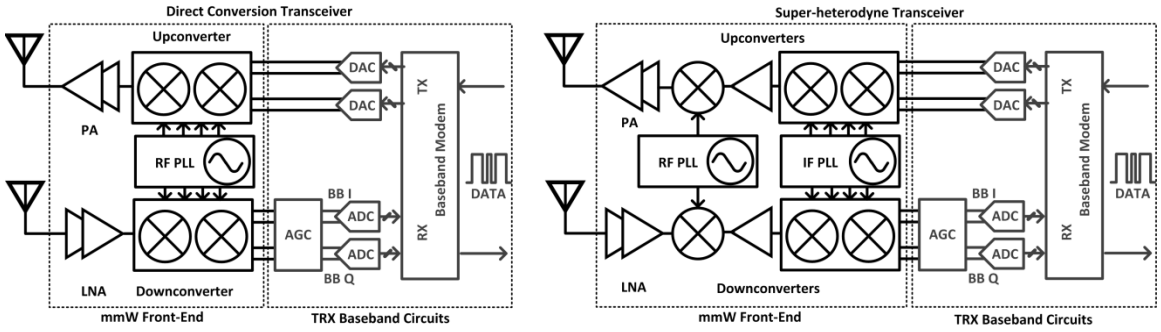


Figure 2.2. Conventional communication transceiver structures include direct conversion and super heterodyne.

The requirements of frequency synthesizers in a wireless transceiver depend on the architecture and the frequency plan. Direct conversion transceivers include one main PLL to down (up) convert baseband signals from (to) RF domain. On the other hand, a super-heterodyne transceiver will separate the conversion into two (or more) steps. A RF PLL and a IF PLL will be used in the system. Individual block, including VCO, dividers, loop filter, and output buffers, can be implemented after the specifications of PLL are

defined. It is significant to design a PLL with an appropriate frequency plan. The required parameters of different PLLs in a RF 60GHz front-end transceiver are shown in Table 2.1.

The benefit of a direct conversion transceiver is its simple system architecture. Only one RF PLL is applied for frequency conversion. No IF amplifiers, mixers, and other PLLs are used, which reduces the complexity of RF systems. On the other hand, the 60GHz RF PLL is more sensitive than the 48GHz one. A same amount of parasitic capacitance or inductance will introduce more frequency shift in VCO. The design has to be utilized carefully to cover the 7GHz bandwidth. Besides, corresponding LO amplifiers will be critical to transmit the 60GHz clock. Large power consumption in the LO path is inevitable. Moreover, a direction conversion communication would require filters to suppress the image signal at the baseband. As a result, the super-heterodyne transceiver is relatively favorable in a more reliable architecture to distribute the design risk in LO and IF circuits than the direct conversion system. With the specifications shown in Table 2.1, the parameters in a PLL can be modeled by the transfer function as the first phase of design.

Table 2.1. The specifications of frequency synthesizers in 60GHz applications: from baseband to RF interface.

System / Spec.	**Super-heterodyne Transceiver**			**Direct Conversion Transceiver**	
PLL required	RF PLL	IF PLL	Baseband PLL	RF PLL	Baseband PLL
Output Frequency	45.36 47.52 49.68 51.84 GHz	12.96 GHz	2.97-3.456 GHz	58.32 60.48 62.64 64.80 GHz	2.97-3.456 GHz
Type	Integer-N	Integer-N	Fractional-N	Integer-N	Fractional-N
Loop Bandwidth	1 – 2 MHz	1 – 2 MHz	100 - 200 KHz	1 – 2 MHz	100 - 200 KHz

Reference Frequency	27 MHz	27 MHz	27 MHz	27 MHz	27 MHz
Division Ratio	1680 1760 1840 1920	480	110 - 128	2160 2240 2320 2400	110 - 120
Application	Frequency conversion (Four channels)	Frequency conversion (Fixed frequency)	ADC, DAC, and baseband signal processing	Frequency conversion (Four channels)	ADC, DAC, and baseband signal processing

The RF PLL has to be locked for four channels, which means the loop should have enough phase margin, locking speed, and similar bandwidth, regardless of the variation of VCO gain and frequency shift. The system may be out of lock when the complexity is increased. Therefore, a programmable PLL is preferred over fixed specifications for phase margin and acquisition speed adjustment.

2.3 Specifications of Frequency Synthesizer

The specifications of PLL include the following:

- Loop dynamics: Phase margin and loop bandwidth define the closed-loop behavior. They affects PLL stability.
- Locking time: It is the time when the loop is settled and the output frequency is locked. It may take a long time for actual phase lock. It provides information of response time and is related to the loop dynamics.
- Locking range: It is the frequency range the PLL can afford.
- Phase noise: It defines the purity of signal in frequency domain.
- Jitter: It defines the purity of signal in time domain.
- Reference spur: It describes the impact of input reference signal on output signal.
- Hardware specifications: It includes power consumption, area, and liability.

PLL generates a clock for data links and modulation in a communication system. The noise specifications, including phase noise, jitter, and reference spur, are important for PLL. They are targeted specifications of this work and will be further explained.

The signal generated by a PLL is ideally sinusoidal, and can be expressed as

$$V_0(t) = A_0 \cos(W_0 + \phi_0), \tag{4}$$

where A_0, W_0, ϕ_0 are constants and present oscillation amplitude, frequency, and phase respectively. On the spectrum, the phase noise is defined as the ratio of noise power in a 1Hz window to the carrier power (main tone) at a specific frequency offset from the carrier [25]. The phase noise can be expressed as

$$\mathcal{L}(w_m) = \frac{Power\ in\ 1Hz\ window}{Carrier\ power} = \frac{S_V(w_0 \pm w_m)}{A_0^2/2} \left(\frac{dBc}{Hz}\right), \tag{5}$$

where w_m is the offset frequency, $S_V(w)$ is the signal power spectrum, and $S_V(w_0 \pm w_m)$ is the one-side noise power at w_m. $\mathcal{L}(w_m)$ is used as single-sideband phase noise. Phase is an integral result of frequency. A slope of a -20dB/decade will appear as one part of phase noise segments shown in Figure 2.3(a). At low offset frequency, the flicker noise in the oscillator device dominates noise distribution and leads to a slope of -30dB/decade. The 1/f flicker noise corner between the two segments is a critical feature of phase noise. Noise distribution after PLL clock is affected by the location of this corner. At high offset frequency, the phase noise will gradually flatten out due to noise floor in the environment. Qualitatively, phase noise is a short-term fluctuation of specified clock in phase domain. In time domain, phase noise is cited as jitter by digital systems and IO designers.

The other significant feature of clock is its spurious tones on spectrum. In a complicated system, there may be supply noise, multiple clocks, and self-multiplication, which all result in harmonics on the spectrum. The spurious level can be quantitatively defined as the ratio of spurious power to carrier power. In a PLL, the clock output is multiple times of reference frequency. Intuitively the reference harmonics should appear on the narrow band spectrum. In time domain, the spurious tone can be realized as an event caused by periodic charge and discharge on the charge pump output. The event modulates the VCO output frequency. The resulting spectrum will include spurious tones at a frequency offset of reference frequency from the carrier as shown in Figure 2.3(b). The spurious level caused by reference clock is called reference spur for a PLL.

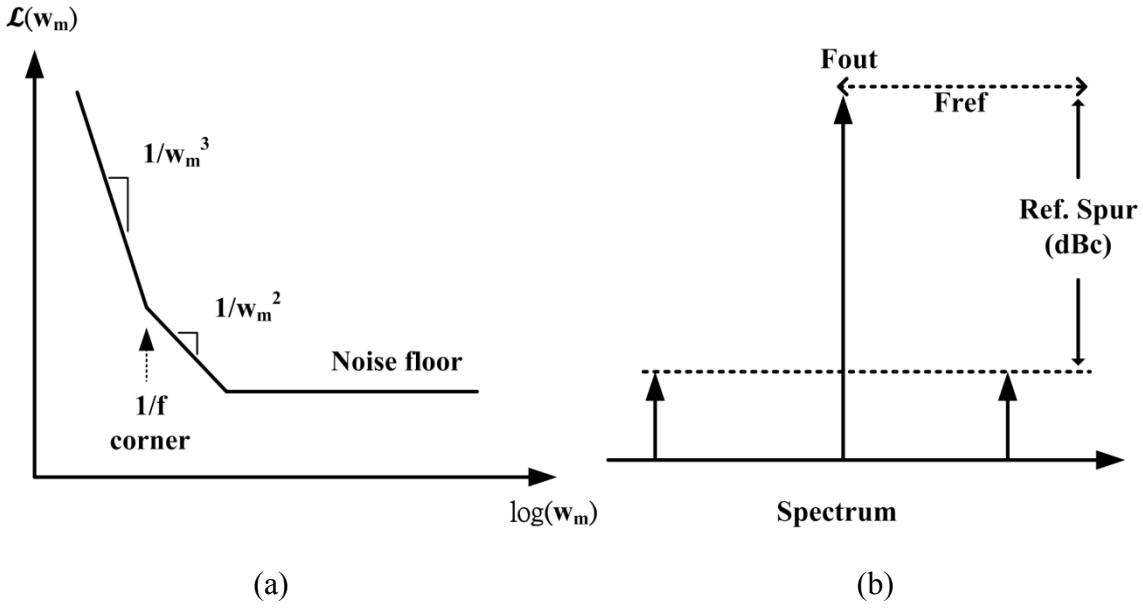


Figure 2.3. (a) The profile of phase noise (w_m) with -30dB/decade and -20dB/decade slopes shows a 1/f frequency corner between the two segments. (b) Reference spur of a PLL output on spectrum.

The reference spur can be derived based on frequency modulation. If an ideal sinusoidal wave is modulating the VCO in reference frequency, the VCO frequency can

be expressed as $w(t)=w_0+\Delta w_0 \cdot \cos(w_{ref}t)$. Since the integral of frequency is phase, the modulated output phase becomes

$$\theta(t) = \int w(t)dt = \theta_0 + \int \Delta w_0 \cos(w_{ref}t)dt = \theta_0 + \frac{\Delta w_0}{w_{ref}} \sin(w_{ref}t), \quad (6)$$

where w_{ref} is the reference frequency, w_0 is main carrier frequency, Δw_0 is the amplitude of frequency modulation, and θ_0 is the initial phase. The fact that $\Delta w_0/w_{ref}$ is small provides small angle approximation on the VCO output signal $V_0(t)$:

$$V_0(\mathrm{t}) = A_0 \cos\left(w_0 t + \theta_0 + \frac{\Delta w_0}{w_{ref}} \sin(w_{ref}t)\right)$$

$$= A_0 \cos(w_0 t + \theta_0) \cos(\frac{\Delta w_0}{w_{ref}} \sin(w_{ref}t)) - A_0 \sin(w_0 t + \theta_0) \sin(\frac{\Delta w_0}{w_{ref}} \sin(w_{ref}t))$$

$$\cong A_0 \cos(w_0 t + \theta_0) - A_0 \frac{\Delta w_0}{w_{ref}} \sin(w_{ref}t) \sin(w_0 t + \theta_0)$$

$$= A_0 \cos(w_0 t + \theta_0)$$

$$- \frac{A_0 \Delta w_0}{2w_{ref}} \cos\left((w_0 + w_{ref})t + \theta_0\right) + \frac{A_0 \Delta w_0}{2w_{ref}} \cos\left((w_0 - w_{ref})t + \theta_0\right). \quad (7)$$

The result shows two tones, $w_0 \pm w_{ref}$, sits at two sides of the carrier, which is exactly the same as the spectrum shown in Figure 2.3(b). The reference spur is then calculated as

$$Reference\ spur = \frac{Power\ of\ the\ reference\ tone}{Carrier\ Power} = \frac{\frac{1}{2}(\frac{A_0 \Delta w_0}{2w_{ref}})^2}{\frac{A_0^2}{2}} = \frac{\Delta w_0^2}{4w_{ref}^2}. \quad (8)$$

On spectrum it is conventionally converted to logarithmic scale.

2.4 State-of-the-art PLL Design, Test, and Calibration Techniques

Design, test, and calibration of frequency synthesizer has been investigated in many publications. In this section, previous achievement and prior art will be introduced based on research focus in the dissertation for further progress and comparison.

The performance of PLL is based on the evaluation of all specifications including frequency range, bandwidth, locking time, phase margin, phase noise, reference spur, power consumption, and area. A qualified performance of baseband PLL design, is estimated with the minimum overhead to save cost for critical front-end circuits. Additional area and power consumption in the circuits are of concern. A summary of prior work is listed in Table 2.2. In the table, the figure of merit (FOM) is a widely used evaluation for PLL performances. The FOM_T is an extended form containing information for tuning range.

Table 2.2. The summary of prior work for baseband PLL reference.

Ref. / Spec.	[26]	[27]	[28]	[29]	[30]
Tech.	0.35um CMOS	65nm CMOS	0.18um CMOS	65nm CMOS	0.13um CMOS
Freq. (GHz)	2.23 - 2.45	3*	3*	3.03 - 3.67	2.55 - 3
Tuning Range (%)	9.4	10	10	19.1	16.2
Supply (V)	1.5, 2	1.2	1.8	1.2	-
Total Power (mW)	16	36	31.7	27.5	14.2
Phase Nose @1MHz (dBc/Hz)	-115	-104	-121	-111	-120

Area (mm^2)	0.85	0.18	1.2	0.9	0.5
Ref. (MHz)	40-50	40	40	26	50(800)
FOM (dB)	170.3	158	175.3	167.1	177.3
FOM_T (dB)	169.8	158	175.3	172.7	181.5

*10 % FTR is used for FOM calculation
-Not provided in the paper

RF PLL plays the role of synthesizing the whole band over carrier frequency, which allocates 6.48GHz bandwidth at 60GHz spectrum. The most challenging issue of RF PLL design in mmW application is the frequency coverage. Hence the circuit performance is mainly evaluated based on the tuning range factor. Power supply rejection is also critical for the circuitry to overcome PVT variation. Table 2.3 shows the performance summary concluding important prior art. The FOM_{ST} is used to evaluate the VCO performances including tuning range and supply rejection in PLL. The equations of FOM FOM_T, and FOM_{ST} are introduced in the following chapter.

Table 2.3. The summary of prior work for RF PLL reference.

Ref. / Spec.	[31]	[32]	[33]	[34]
Tech.	130nm Si-Ge BiCMOS	65nm CMOS	45nm CMOS	32nm SOI
Freq. (GHz)	15.95 – 18.81	17.5 - 20.94	21.69 - 27.85	21.8 – 27.5
Tuning Range (%)	16.5	17.9	24.9	22.9
Phase Noise @1MHz (dBc/Hz)	-102	-100	-101	-110*

Ref. Spur (dBc)	< -60	< -50	-50	-
Reference Freq. (MHz)	285.714	36	48	-
Supply (V)	1.2, 2.7	1.2, 1.8	0.9, 1.1, 1.8	0.7 - 1.5
Total Power (mW)	144	80	40	36
Area (mm^2)	0.65x1	1.1x1	0.48x0.29	-
PSRR (dB)	< -50	-	-	-
FOM (dB)	-165.2	167.4	172.8	182.3
FOM_{ST} (dB)	172.06	172.5	180.7	189.5

*Calculated assuming 20dB/decade degradation with offset frequency
-Not provided in the paper

Alternate Testing has been used for extract DUT response by sampling low frequencies waveforms with an A/D converter. The digitized response is analyzed externally to establish the mapped feature between response and specifications. The methodology is shown in Figure 2.4 with a statistical regression model for mapping the response. In [19-20], built-in test is implemented using this methodology for low-noise amplifier (LNA), which is a breakthrough in testing in RF components. Input third intercept point (IIP3), 1dB compression point (P_{1dB}), gain, and noise figure (NF) are evaluated for tested RF circuitry with a high accuracy. However, the methodology is never applied for frequency synthesizer that contains a closed loop. An effective response can be achieved by providing adequate stimulus and detecting the useful output features. In this dissertation the analysis and experiment are performed.

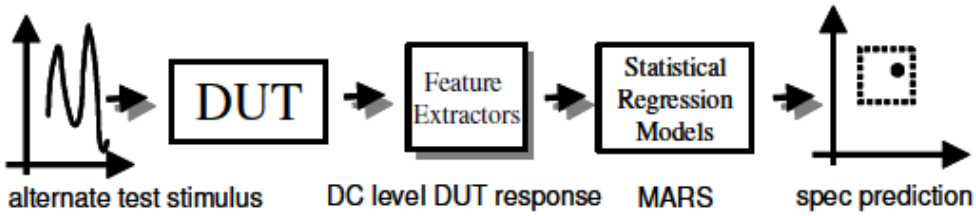


Figure 2.4. Alternate test methodology

In [35], a digital BIST is proposed for PLL loop parameter measurement. Loop gain, lock time, and lock range are the three main loop specifications that are tested. Digital frequency counters are used to measure VCO output frequency variation, and programmable delay circuits are used to adjust PLL input phase. Equations are derived for loop gain, frequency variation, and input phase offset. Lock time is measured by interrupting the loop and counting the number of reference cycles until the input phases are re-aligned. Lock range is estimated in an open loop test configuration from VCO output frequency. These methods require the use of digital circuitry and backend calculations.

The purpose of calibration in a PLL is to optimize the performances and enhance circuit reliability. A target specification has to be first detected by calibration circuits. The circuit should feedback a control signal to adjust the response of the specification after detection. Frequency calibration is a widely used method in a PLL to correct VCO settings for sub-band selection. In this application, the frequency coverage of VCO is divided into sub bands for noise and stability consideration. The techniques can be categorized into closed-loop and open-loop calibration.

In a closed-loop calibration, the loop is first locked for a preliminary comparison [36]. The calibration circuit then decides if the current setup is corrected based on the comparison result. The input voltage of VCO is often used as an comparison index. If it is

not preferred after comparing with a reference, the logic in the calibration will unlock the loop and generate an adjustment on the setup to repeat the detection. The time efficiency is low for this method since the PLL has to be settled for each setting.

An open-loop calibration turns off the loop operation and directly feeds a predefined signal into a PLL for comparison purpose [36]. In this case, a voltage is provided to VCO for test. Comparison then happens between the divided clock and reference clock. The correction will end when the setup is optimized for the comparison. One prior art applies period-based techniques to speed up the calibration time in an open loop [21]. A time-to-voltage converter is used to extract time information for each period so that a fast calibration can be achieved.

Frequency calibration is investigated widely because the exact frequency can be observed directly in digital manors at a divider output. On the other hand, calibration for non-linear effects in a circuit is subtle and difficult. There is no apparent index that can be detected easily for noise. In PLL reference spur is resulted from periodic events in frequency comparison. A prior work tries to reduce the effect by modulating the comparison sequences, but it still faces difficulties in implementing delicate delay circuits and a closed-loop operation [37]. A calibration process on noise means detecting and manipulating noise in a certain range, which are two hard topics. The calibration circuits are hence challenging and meaningful in optimizing non-linear effects in a PLL. A RF system can also gain benefits from the noise information and quality optimization.

CHAPTER 3: FREQUENCY SYNTHESIZER DESIGN

3.1 Fundamentals of Loop Dynamics

3.1.1 Bandwidth and Stability

The implementation of a frequency synthesizer involves not only circuit design but also system development including stability analysis, feedback control, and specification correlation. The open-loop transfer function of a PLL is expressed in Equation (3) previously. The parameters in the equitation should be able to provide the system a stable phase margin above 48 degree [25]. The analysis of loop dynamics can be modeled in Matlab. Design specifications of a baseband 3.456GHz PLL in the following section are used to demonstrate the transfer function, which is shown in Figure 3.1. A third-order loop filter is implemented in the PLL with a bandwidth of 200 KHz and a phase margin of 60 degree.

A closed-loop response of a system is obtained by its open-loop response and feedback factor. Based on Equation (3), the close-loop response is written as

$$H_{cl}(s) = \frac{A}{1 + A \cdot B} = \frac{\frac{H_{ol}}{B}}{1 + H_{ol}} = \frac{N \cdot H_{ol}}{1 + H_{ol}} = H_{REF}(s), \tag{9}$$

where A is the open-loop response, B is the feedback factor, and N is the division ratio when a integer-N PLL is considered. Equation (9) is the response from the input signal, which equivalently evaluates the noise impact from reference signal to output signal in the loop. The effective phase noise from reference clock to output clock can be calculated by multiplying reference phase noise by Equation (9). To obtain PLL output phase noise, the noise interference from different block has to be considered as shown in Figure 3.2.

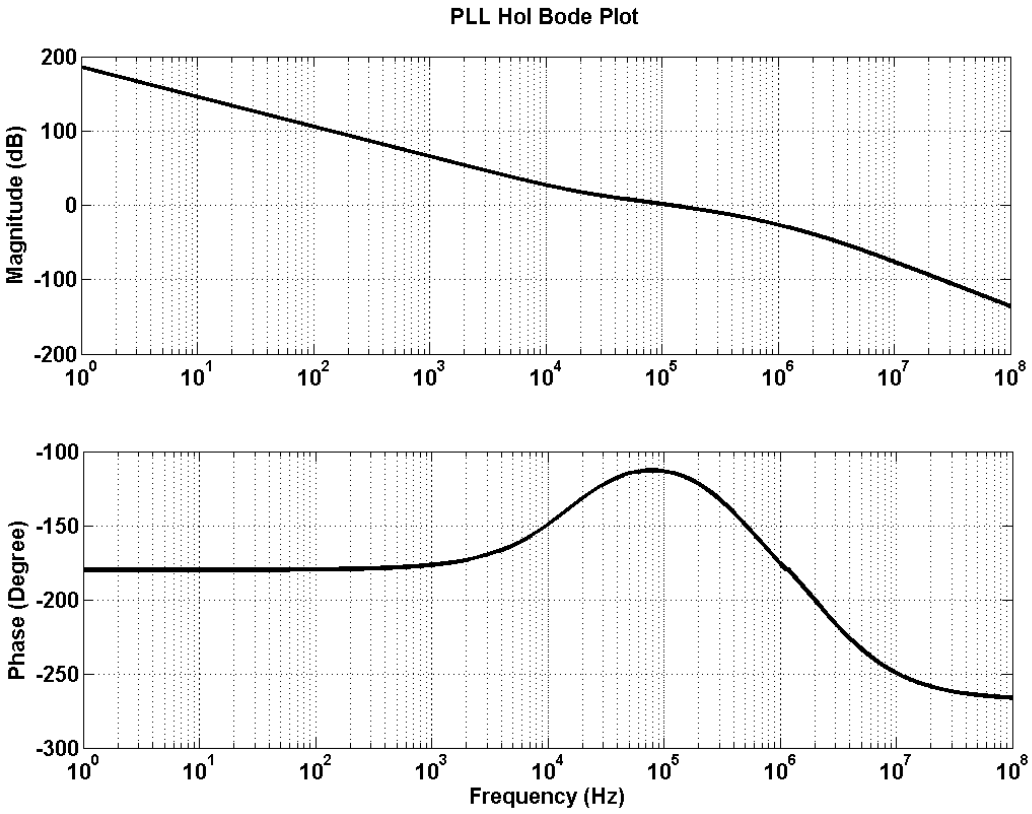


Figure 3.1. The bode plot of PLL open-loop transfer function shows a bandwidth of 200KHz and a phase margin of 60 degree.

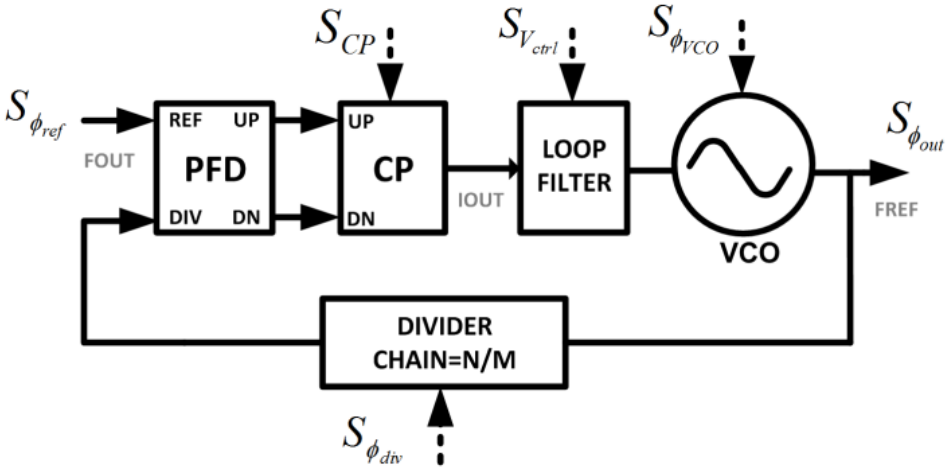


Figure 3.2. The overview of noise inputs from different blocks in a PLL loop.

The closed-loop transfer function of different inputs can all be calculated in a similar way for the reference clock. By superposition, the overall phase noise can be summed together. The most dominant effects are actually the VCO and reference phase noise. The transfer function of noise at VCO can be express as

$$H_{VCO}(s) = \frac{1}{1 + H_{ol}}. \tag{10}$$

The overall phase noise S_{out} can be expressed as

$$S_{\phi_{out}} = S_{\phi_{ref}} \cdot |H_{REF}(s)|^2 + S_{\phi_{VCO}} \cdot |H_{VCO}(s)|^2, \tag{11}$$

where S_{REF} and S_{VCO} are the phase-noise profile in a linear scale of power level. When calculating the phase noise, it is expressed logarithmically with respect to the carrier. The unit of phase noise is dBc per Hertz. Figure 3.3 is an example of overall phase noise estimated based on VCO, reference phase noise, and transfer function. The profiles of phase noise are obtained from a measured 27MHz crystal oscillator and a 3.456GHz LC-VCO in CMOS 65nm.

In the process of implementing frequency synthesizers, it is necessary to understand the loop dynamics and decide the parameters in a stable method. The specifications of PLLs in different frequency domains (RF, IF, and baseband) of a 60 GHz transceiver will be introduced. A programmable technique for PLL acquisition speed will then be proposed.

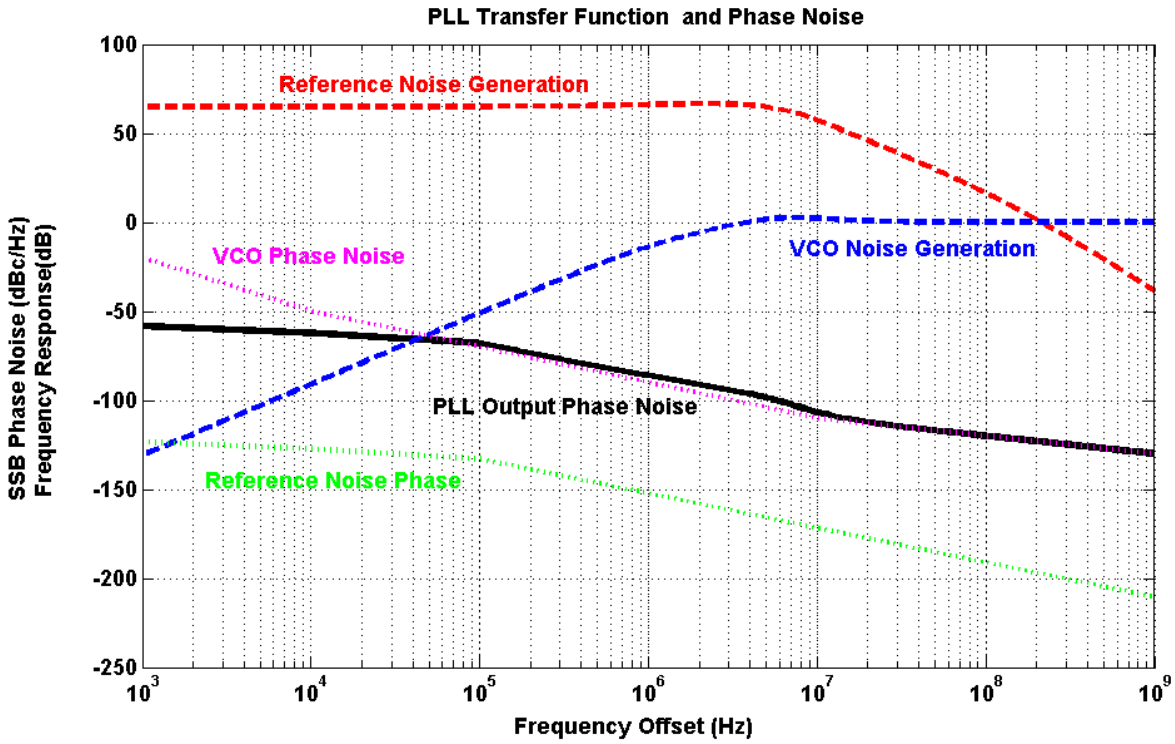


Figure 3.3. The overall phase noise is the total effect from reference noise and VCO noise. The dotted lines are the phase noise profile and corresponding transfer function.

3.1.2 Adaptable Acquisition Speed

For low data rate communication, such as Bluetooth, the frequency hopping requirement is low. The synthesized PLL frequency can stay in a channel for a long period of time. The timing specification is normally above 100 usec, which provides an maximum value for the PLL acquisition speed. However, the requirement of multi-gigabit data transmission is more stringent because more bits are transmitted in a shorter burst period than low data rate transmission.

One of the critical problems in millimeter-wave design is the frequency characterization. The frequency of a VCO can vary significantly after manufacturing. Most of the PLL designs [32-33], utilize the capacitance banks to cover the target wide frequency bands by fine adjustment. However, these capacitance banks will be affected

by parasitic variation and create unevenly distributed tuning curves and K_{VCO} in a high frequency VCO. The result therefore leads to different behaviors of acquisition speed and loop dynamics.

This section proposes a RF frequency synthesizer design with programmable loop parameters. The technique requires implementations of an adaptive charge pump and a reconfigurable loop filter. The programmability provides flexibility and margin for a high frequency PLL so that it can adjust the acquisition speed and achieve a fast locking.

The structure of a third-order charge pump PLL is used and shown in Figure 3.4. A PLL design involves the consideration of loop bandwidth, locking time, and stability. A narrow loop bandwidth benefits the system with better spur levels at the expense of a long locking time. In the multi-gigabit application, the channel spacing is larger than 2 GHz, and the impact from reference spur is less significant than narrow band application. The loop bandwidth and phase margin can be obtained from the PLL open loop transfer function (Equation (3)). The transimpedance of loop filter Z(s) can be expressed as

$$Z(s) = \frac{1 + sC_1R_1}{s(A_0 + sA_1 + s^2A_2)}, \tag{12}$$

where $A_0=C_1+C_2+C_3$, $A_1=C_1R_1(C_2+C_3)+C_3R_3(C_1+C_2)$, and $A_2=C_1C_2C_3R_1R_3$. The third order loop filter has a pole at the origin. R_1 and C_1 generate a zero, W_z. When $C_1 >> C_2$, C_3, and $R_1 > R_3$, the second pole, W_{p2}, is approximately decided by R_1 and C_2+C_3 [6]. The PLL loop bandwidth is equal to the open loop unity gain bandwidth, Wu, which should be designed between W_z and W_{p2} for a better phase margin. The ratio of W_z to W_{p2} decides the phase margin when Wu equals to the geometric mean of W_z and W_{p2}. R_3

and C_3 are carefully chosen to generate the third pole for extra spur suppression. The overall PLL transfer function contains another pole at the origin from the VCO.

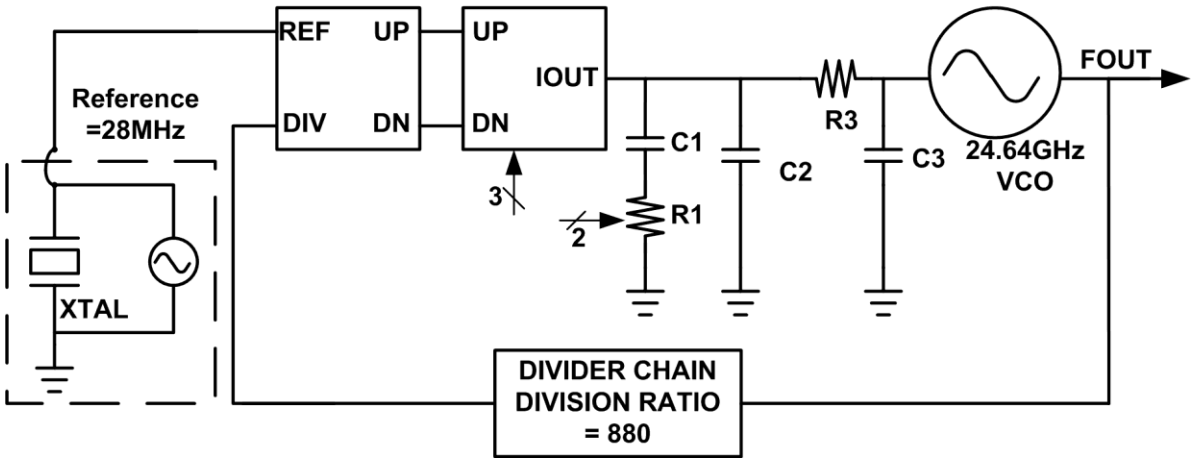


Figure 3.4. The 24GHz frequency synthesizer design with adaptable loop control.

VCO gain (K_{VCO}) will vary for different tuning curves due to parasitic effects. From Equation (3), the open loop gain of PLL will be changed when K_{VCO} is varied. The loop bandwidth and phase margin are no longer fixed either. Therefore the charge pump current and the loop filter transimpedance are adjusted to compensate the variation and maintain the same loop behavior. Before starting circuit design, it is essential to analyze the effect of the two aforementioned variables. The loop filter transimpedance, Z(s), has passive components. In general, the location of the zero, W_z, has a dominant effect on the loop bandwidth and phase margin. To change the zero, either the resistor, R_1, or the capacitance, C_1, has to be changed. R_1 is used due to area concern.

The bode plots of PLL open loop transfer function are shown in Figure 3.5 to illustrate the effect of changing charge pump current, I_{CP}, and the resistor, R_1.

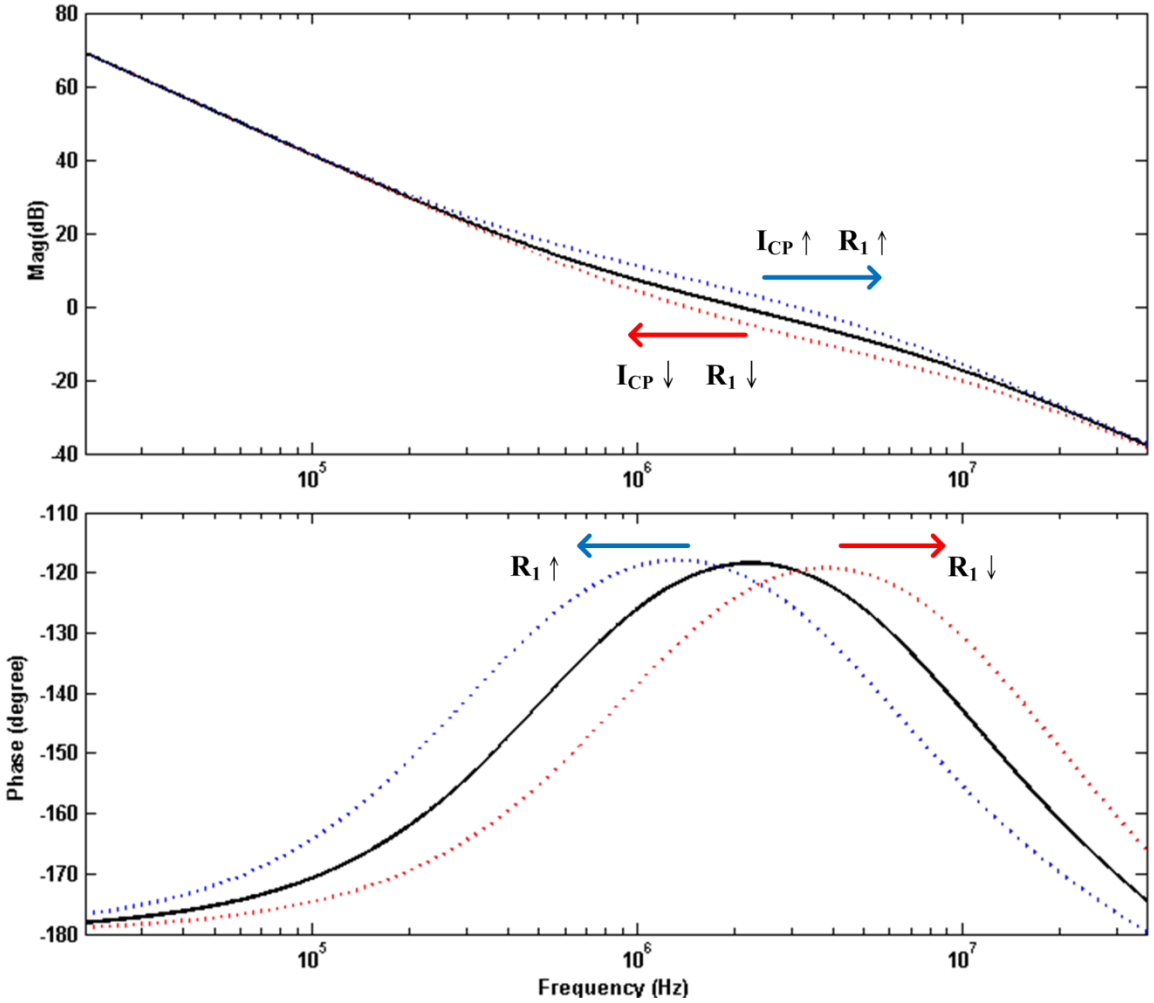


Figure 3.5. The movement of magnitude and phase response of PLL open loop transfer function when charge pump current I_{CP} and resistor R_1 are changed.

The open loop gain is increased when increasing I_{CP}. The loop bandwidth then moves toward high frequency with the phase response maintained. This is because I_{CP} has no effect on Z(s), which is the only factor determining the phase. Similarly, as I_{CP} is decreased, the loop bandwidth drops. Consequently, the loop bandwidth is shifted proportionally to I_{CP}, while the phase margin degrades. On the other hand, both magnitude and phase response would be modified when controlling R_1. It can be realized by moving the location of the zero. A large value of R_1 means a small W_z but W_{p2} is kept unchanged at the same time. The magnitude response moves toward high frequency and

the phase response moves toward low frequency. The loop bandwidth then increases with a reduced phase margin because of the opposite pulling directions on the magnitude and phase. As a result of moving R_1, the loop bandwidth is shifted proportionally but the phase margin degrades. The variation is worse than the condition of changing I_{CP}.

There is a limit on the loop bandwidth programmability when I_{CP} and R_1 are too large or too small. The degraded phase margin would lead to instability. A better way to control the loop is to vary the other parameter in opposite directions so that the phase margin can be compensated accordingly. For example, a large charge pump current and a small resistor can simultaneously increase the loop bandwidth and maintain a good phase margin.

The schematic of the programmable third-order loop filter is shown in Figure 3.6. Four switches are used to change the resistor values of R_1. A two-to-four decoder is implemented for the two-bit control. Inside the loop filter, C_1 is 40 pF, C_2 is 1 pF, R_3 is 1 KΩ, and C_3 is 1.5 pF. R_1 is 7 KΩ for a default loop bandwidth of 2 MHz and a phase margin of 61.5 degree. The gain of VCO (K_{VCO}) is 1.4 GHz/V. Programmable resistor values are 4 KΩ, 12 KΩ, and 20 KΩ respectively. When only the main resistor, R_1, is changed, the loop bandwidth can be controlled from 1.4 MHz to 3 MHz with a phase margin larger than 49 degree. A large-sized transistor is required for the switch to reduce the injected noise. The parasitic capacitance of switches is relatively small compared with the main capacitance, C_1. In simulation, the parasitic capacitance of a switch is less than 100fF, which is 0.25 % of C_1 and can be ignored.

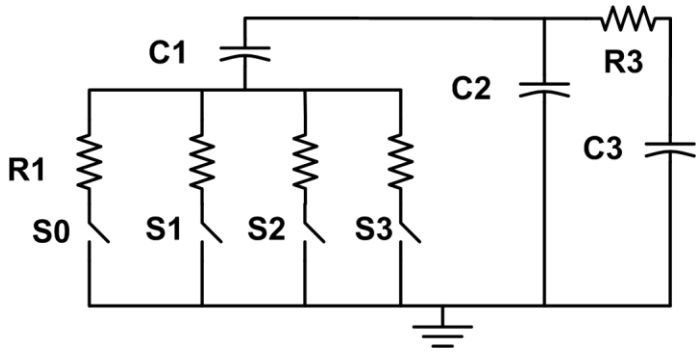


Figure 3.6. The loop filter with programmable zero location

The charge pump design, which adopts the complimentary UP and DN signals for a balanced output current, is shown in Figure 3.7. M5 and M8 are current output stages. M9 and M10 are used to keep the output common-mode voltage from periodic variation of charging and discharging activities. M11 to M14 compensate the effects of charge sharing and charge injection. The eight switches from S0 to S7 provide the programmability on charge pump current. The IPTAT (current proportional to absolute temperature) provides an ability to track the transconductance variation on transistors against the PVT variation. A three-to-eight decoder is adopted for the three-bit control of current. I_{CP} is designed to be 1.2 mA with a configurable range from 200 uA to 1.7 mA. When only I_{CP} is changed, the loop bandwidth can be controlled from 0.8 MHz to 2.8 MHz with a phase margin larger than 49 degree.

A 1-V 24GHz synthesizer is designed in TSMC 65nm CMOS technology. The total current consumption is 25 mA. The K_{VCO} is 1.4 GHz/V.

The adjustable range of loop bandwidths and phase margins are listed in Table 3.1. As mentioned above, a simultaneous adjustment of I_{CP} and R_1 helps keep a better phase margin (> 54 degree) for the loop stability. In the case of varying I_{CP} or R_1 only, the phase margin has more degradation (< 50 degree). As a result of programming, the

24GHz synthesizer has a loop bandwidth from 0.94 MHz to 2.05 MHz and a phase margin better than 54 degree. In some cases, the loop cannot reach its steady state fast enough even when a wide loop bandwidth is used. This is because the phase margin is small and creates instability for the loop. A phase margin that is smaller than 50 degree will lead to damping behaviors on the VCO control line.

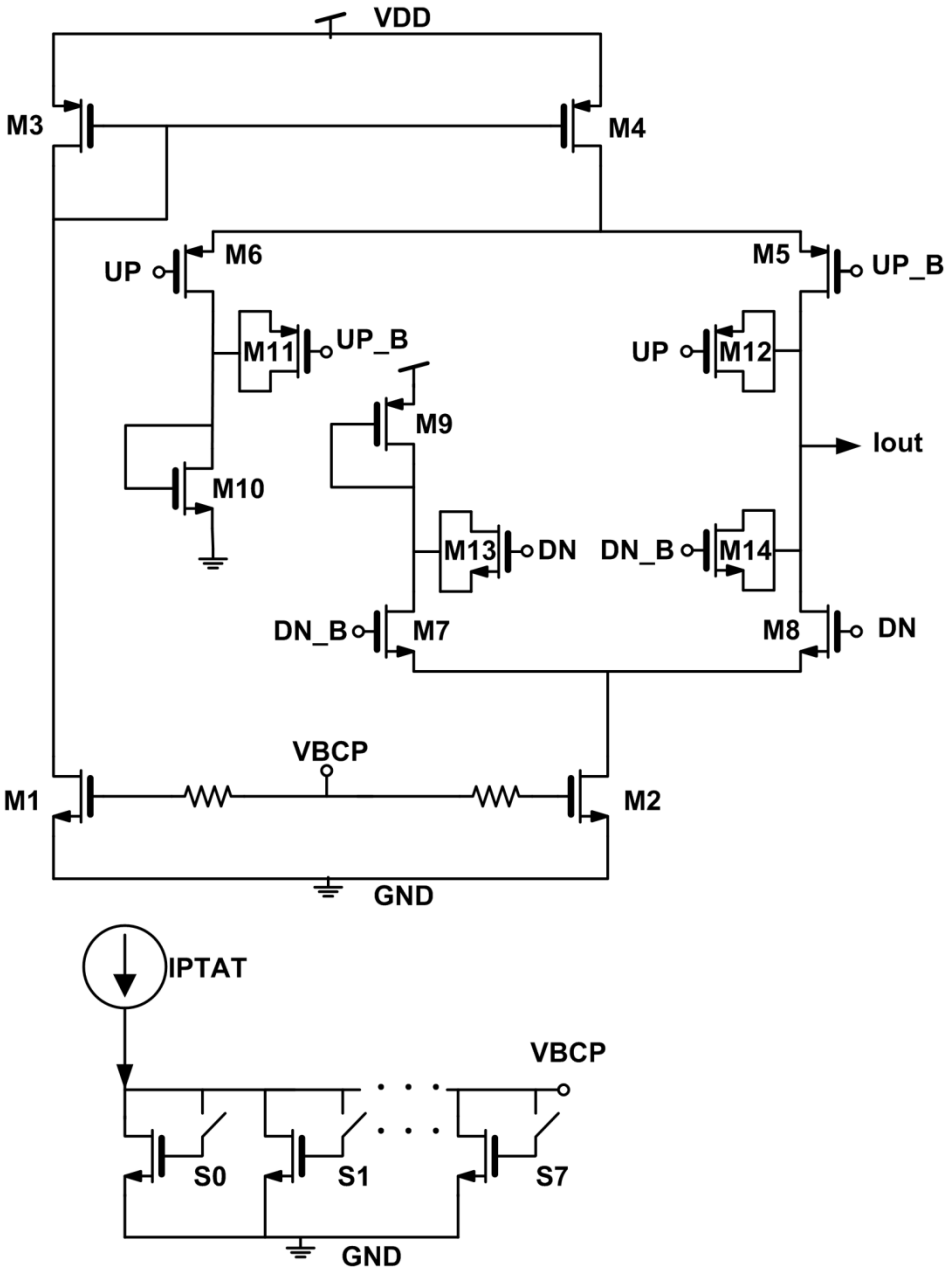


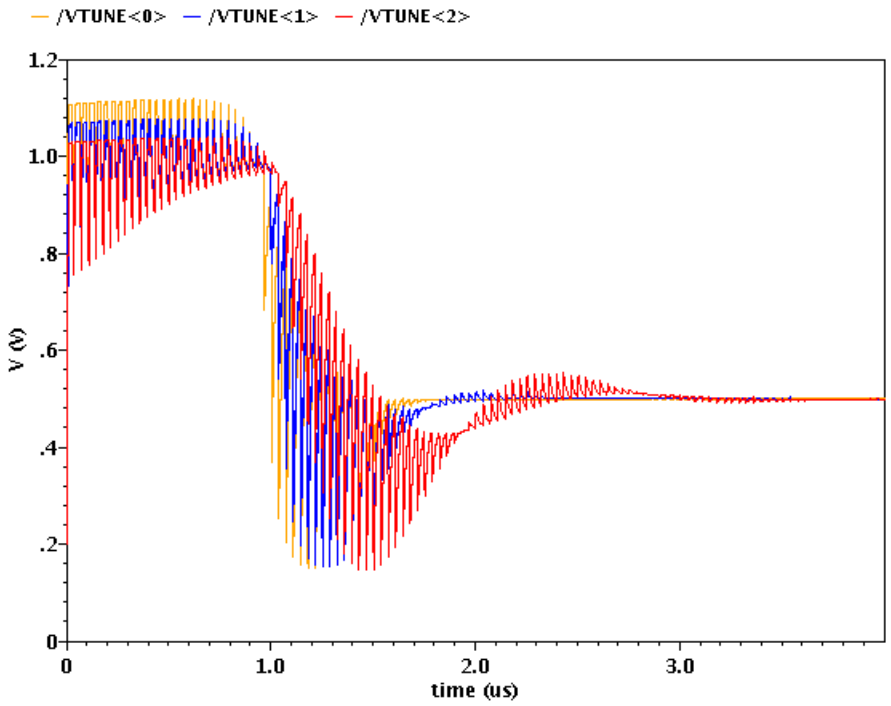
Figure 3.7. The charge pump design with programmable diode-connected current mirrors.

Table 3.1. Adjustable range of PLL loop parameters.

I_{CP} (mA)	R_1 (KΩ)	W_u (MHz)	PM (°)
1.2	7	2.05	61.5
1.7	4	1.84	54.6
0.2	20	0.94	62
1.2	4	1.4	49.1
1.2	12	3	54
0.4	7	0.8	49.6
0.8	7	1.43	59.2
1.7	7	2.8	61

The simulation results of corresponding locking time of PLL when the loop bandwidth is varied from 0.94 MHz to 2.05 MHz are shown in Figure 3.8(a). The acquisition speed is in the range from 1.75 μs to 3.5 μs.

Different VCOs are also used in this PLL design to verify the tolerance for different gain values. VCOs with K_{VCO} equal to 1 GHz/V and 2 GHz/V are placed in the synthesizer for comparison respectively. When the K_{VCO} is 1 GHz/V, the settling time of loop can be reduced from 2.68 μs to 2.36 μs by changing I_{CP} from 1.2 mA to 1.7 mA as shown in Figure 3.8(b). In the case when K_{VCO} is equal to 2 GHz/V, a 16% reduction of locking time can be achieved by varying R_1 from 7 KΩ to 4 KΩ and varying I_{CP} from 1.2 to 1.7 mA. The case with K_{VCO} equal to 1.4 GHz/V is shown in Figure 3.8(c). The locking time is changed from 1.86 μs to 1.57 μs. The phase noise of VCO at 24 GHz is -92dBc/Hz at 1MHz offset with K_{VCO} equal to 1.4GHz/V.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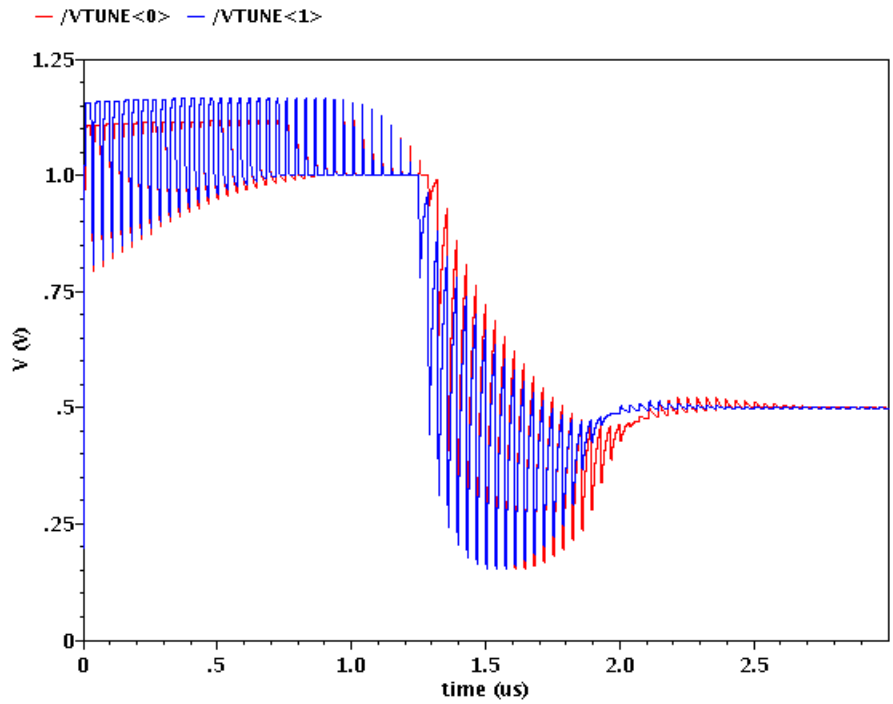
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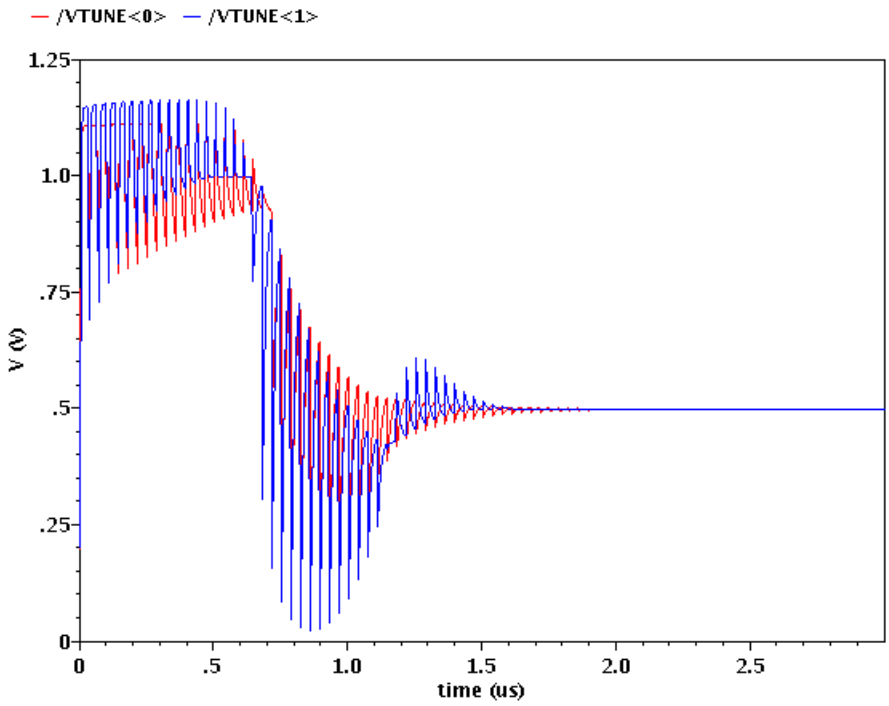


(c)

Figure 3.8. (a) Acquisition speed of PLL for K_{VCO} of 1.4 GHz/V can be controlled from 1.75 µs to 3.5 µs (loop bandwidth from 2.05 to 0.94 MHz) by adjusting I_{CP} and R_1. (b) Acquisition speed for K_{VCO} of 1 GHZ/V can be controlled from 2.68 µs to 2.36 µs, which is 12 % faster. (c) Acquisition speed for K_{VCO} of 2 GHZ/V can be controlled from 1.86 µs to 1.57 µs, which is 16 % faster.

These three VCOs (with K_{VCO} equal to 1 GHz/V, 1.4 GHz/V, and 2 GHz/V) are used to demonstrate compensation on locking time. Through a proper trimming, the locking times for the three loops can be adjusted to a similar value. In Figure 3.9, the simulation results of the locking curves before and after loop adjustment are shown. For the loop with 1GHz/V K_{VCO}, the charge pump current is increased from 1.2 to 1.7mA in order to raise the response speed. For 1.4 GHz/V and 2GHz/V K_{VCO}, the charge pump current is decreased to 0.8 mA and 0.4 mA respectively, to slow down the loop response. As a result, the locking times for the three cases are 2.29 µs, 2.32 µs, 2.36 µs. The

maximum variation is 70ns, which is small and shows the compensation on K_{VCO} difference in high frequency applications.

In summary, a 1V 65nm CMOS 24GHz synthesizer is designed with adaptive control on the loop parameters. Adjustment of the acquisition speed under different conditions can be achieved. This technique allows a frequency synthesizer used for millimeter-wave multi-gigabit applications to be fast-locked and flexible on the acquisition speed against PVT variation.

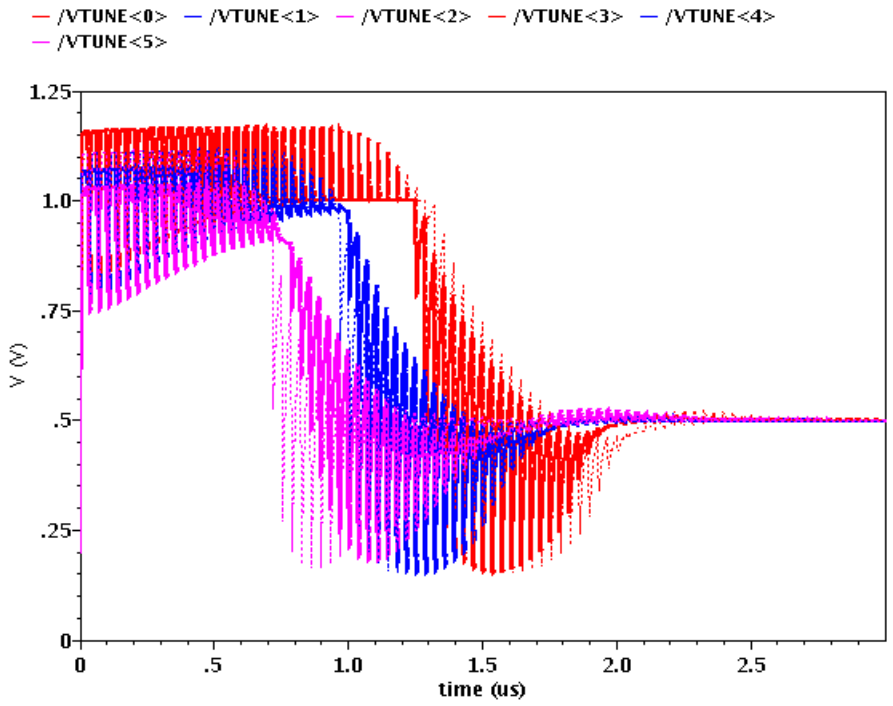


Figure 3.9. Acquisition time of PLL with K_{VCO} equal to 1, 1.4, and 2GHz/V. The speed can be adjusted to 2.36 µs, 2.32 µs, and 2.29 µs from 2.68 µs, 1.75 µs, and 1.86 µs respectively. Dotted lines are control curves before alteration while solid lines are curves after alteration.

3.2 Frequency Synthesizer in Baseband

3.2.1 Area Reduction and Internal Reference Generation

This section presents a CMOS 65nm sigma-delta frequency synthesizer with an embedded capacitor multiplier to support multi-gigabit communication in millimeter-wave transceivers. The capacitor multiplier achieves an equivalent capacitance value of 540 pF and saves 90 % of area for the main capacitor. The multiplier is optimized for VCO noise performance with a phase noise of -117 dBc/Hz at 1MHz frequency offset of 3.456GHz carrier. The current consumption of the multiplier is 327 uA. The VCO is centered at 3.5 GHz with a frequency range of 1 GHz to supports multiple data rates (3.52 Gbps, 3.456 Gbps and 2.97 Gbps) in IEEE 802.15.3c. Moreover, a flexible reference frequency from 10 MHz to 40 MHz can be used because of the feature of the fractional-N architecture. The adjustable reference frequency provides additional design margin for system integration. With this area efficient and reference flexible design, the synthesizer can be integrated into the 60GHz transceiver as a baseband solution.

One of previous 60GHz radio transceiver designs [38] utilizes a PLL based on ring oscillator for transmitter and receiver baseband operation. The approach occupies small area and consumes small current but has the disadvantage of poor phase noise (about -90dBc/Hz at 1MHz frequency offset of 3.456GHz). There are two drawbacks. One is the higher noise level, which hardly supports high-order modulation schemes compared with a LC-VCO. The other is based on system requirement. More than one crystal oscillator will be used when other standards or applications exist in a large-scale integrated communication system. The proposed fractional-N PLL with LC-based VCO supports data rates of 3.456/1.728 Gbps and 3.52/1.76 Gbps (WiGig [7] and WirelessHD

[8]) for 60GHz millimeter-wave wireless transceivers. LC-VCO can generate a stable output frequency for a high level modulation. Moreover, a capacitor multiplier is embedded in the loop filter for area efficiency. Different reference frequencies ranging from 10 MHz to 40 MHz are acceptable for integration purpose when different specifications are applied.

The block diagram of the frequency synthesizer is shown in Figure 3.10, which is a third order sigma-delta fractional-N PLL adopting input reference frequency from 10 MHz to 40 MHz. In sigma-delta PLL designs [26,39-40], the characteristic of noise shaping leads to a narrow bandwidth requirement for noise reduction. An active loop filter with capacitor multiplier is designed to achieve bandwidth reduction and quantization noise filtering from modulator. The utilized area is also efficient due to the capacitance multiplication.

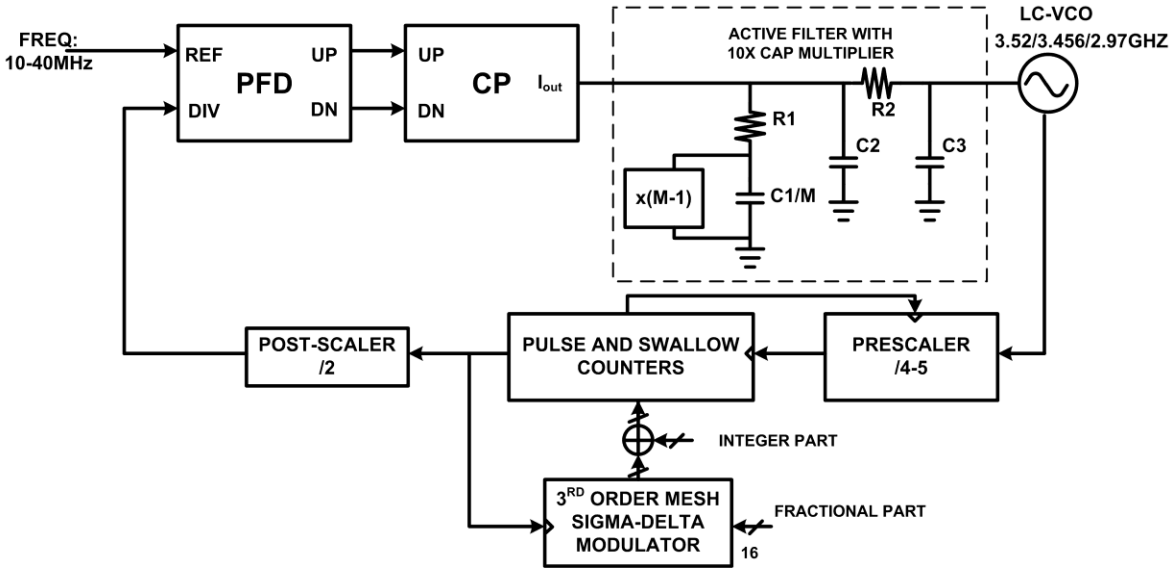


Figure 3.10. The sigma-delta fractional-N frequency synthesizer with a capacitor multiplier for baseband integration.

The other advantage of this PLL is to synthesize an internal reference clock as shown in Figure 3.11. The high frequency clock is divided down to attain a phase noise

better than -150 dBc/Hz (at 1MHZ offset) for reference frequency domain. It can be distributed as a fixed and clean reference signal for millimeter-wave and IF PLL in a super-heterodyne system.

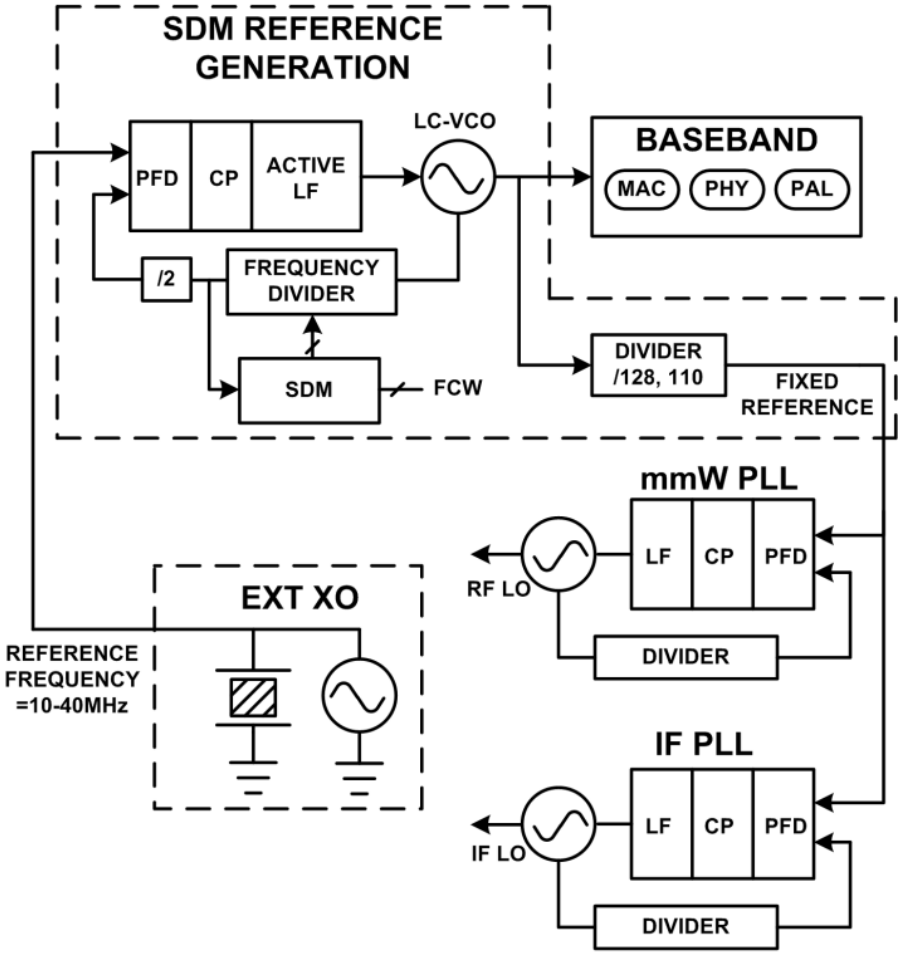


Figure 3.11. Integration of reference generation with a mmW transceiver.

The designed bandwidth of loop filter is located at 100 KHz. The details of circuit implementation are described in the following sections.

3.2.2 **Building Blocks**

The charge pump schematic is shown in Figure 3.12 with current mismatch and glitch suppression. The operational amplifier features a rail-to-rail characteristic to cover

the output common-mode voltage range. The transmission gates are served as signal buffers in up/down paths to match the delay of inverters. The amplifier A enforces the voltages of CP output and Vm to be the same so that the mismatch between charging and discharging current is reduced. The amplifier B enforces the voltage of CP output and Vd to be the same for switching balance. Four dummy transistors are half size of control transistors to eliminate the current injection effect.

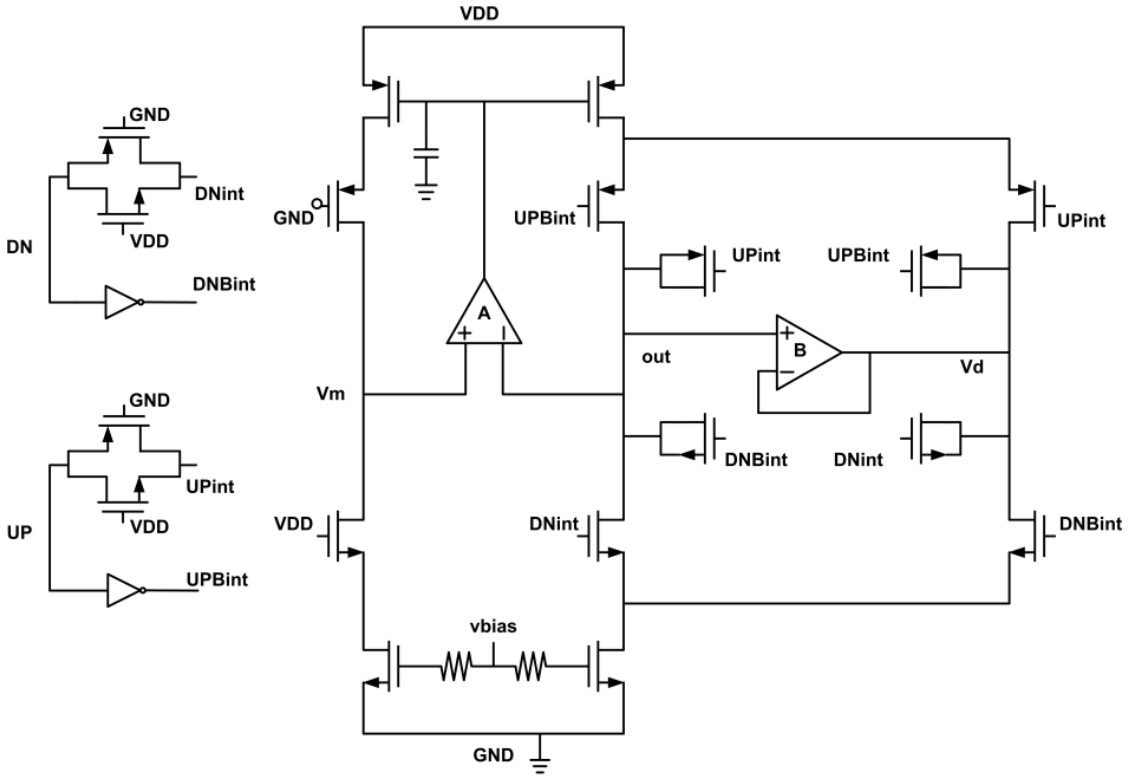


Figure 3.12. Schematic of charge pump with mismatch and glitch suppression.

The utilized programmable frequency divider features the pulse-swallower architecture shown in Figure 3.13. The divide-by-4/5 prescaler can operate at a highest frequency of 3.52 GHz. The divider is directly coupled from the LC-VCO. The overall division ratio is N. N is equal to P·M+S, where P, S, and M represent, respectively, the division ratio of pulse counter, swallow counter and prescaler. In order to minimize the

power consumption and increase the bandwidth of dividers, the prescaler is implemented in true single phase clock (TSPC) topology shown in Figure 3.14.

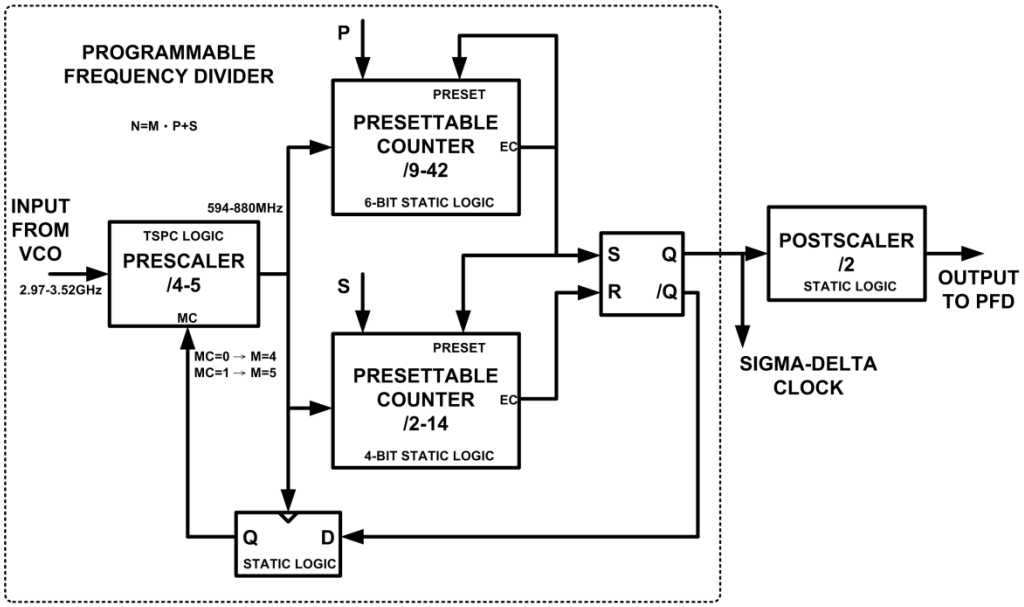


Figure 3.13. Architecture of the programmable frequency divider.

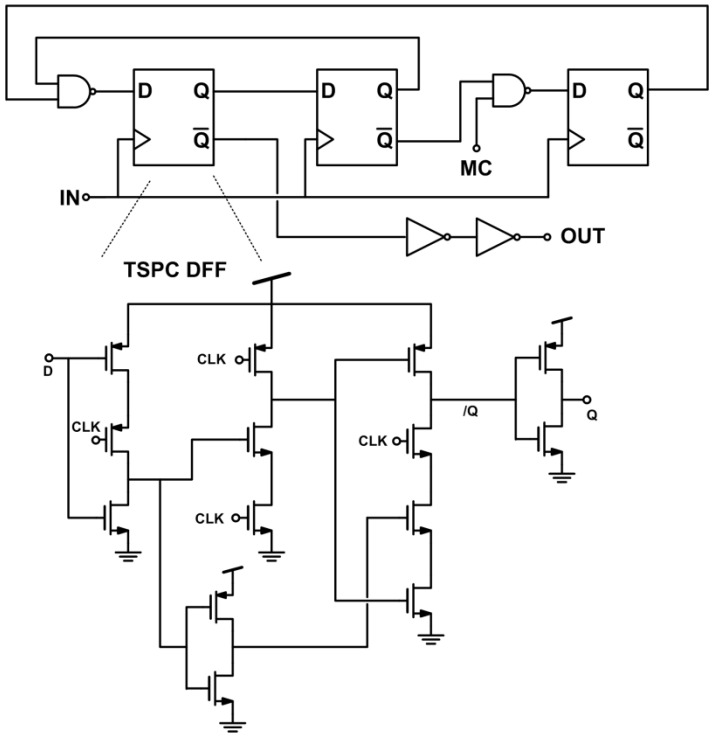


Figure 3.14. Schematic of the divide-by-4/5 TSPC prescaler.

A third order 1-1-1 mesh structure is used for the sigma-delta modulator as shown in Figure 3.15. The modulator controls the fractional part of division factor and scrambles the division sequence. A high-pass shape of phase response will be shown on PLL spur spectrum. Therefore, a narrow bandwidth of PLL is required for noise reduction.

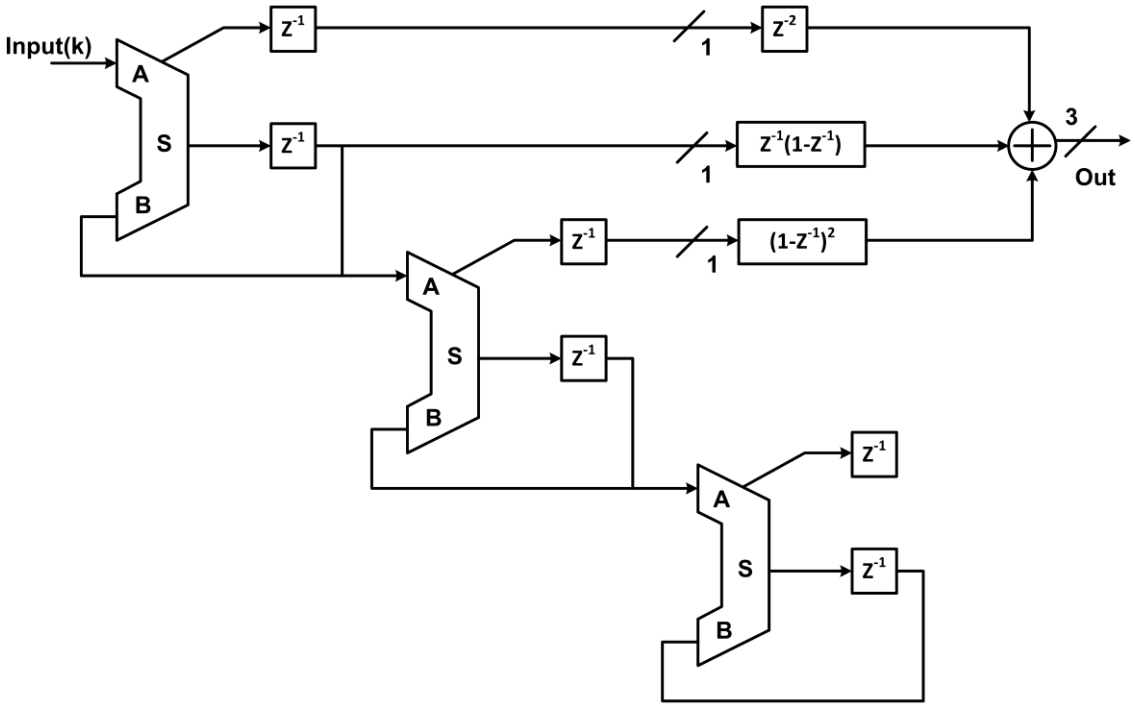


Figure 3.15. Schematic of 3rd order 1-1-1 mesh sigma-delta modulator.

The requirement for low phase noise (-120 dBc/Hz @ 1MHz offset) mandates particular attention to the VCO noise up-conversion from the current source. After extensive simulation, the topology of choice is the NMOS cross-coupled with center-tapped inductor shown in Figure 3.16 To cover the required tuning range over PVT, a programmable capacitors bank has been included. The supply purity is of concern. Noise from supply to the VCO will introduce relevant noise through the VCO current source modulation. The proposed solution includes a simple unity-gain feedback voltage regulator introducing 27 dB of PSRR to suppress the noise from supply.

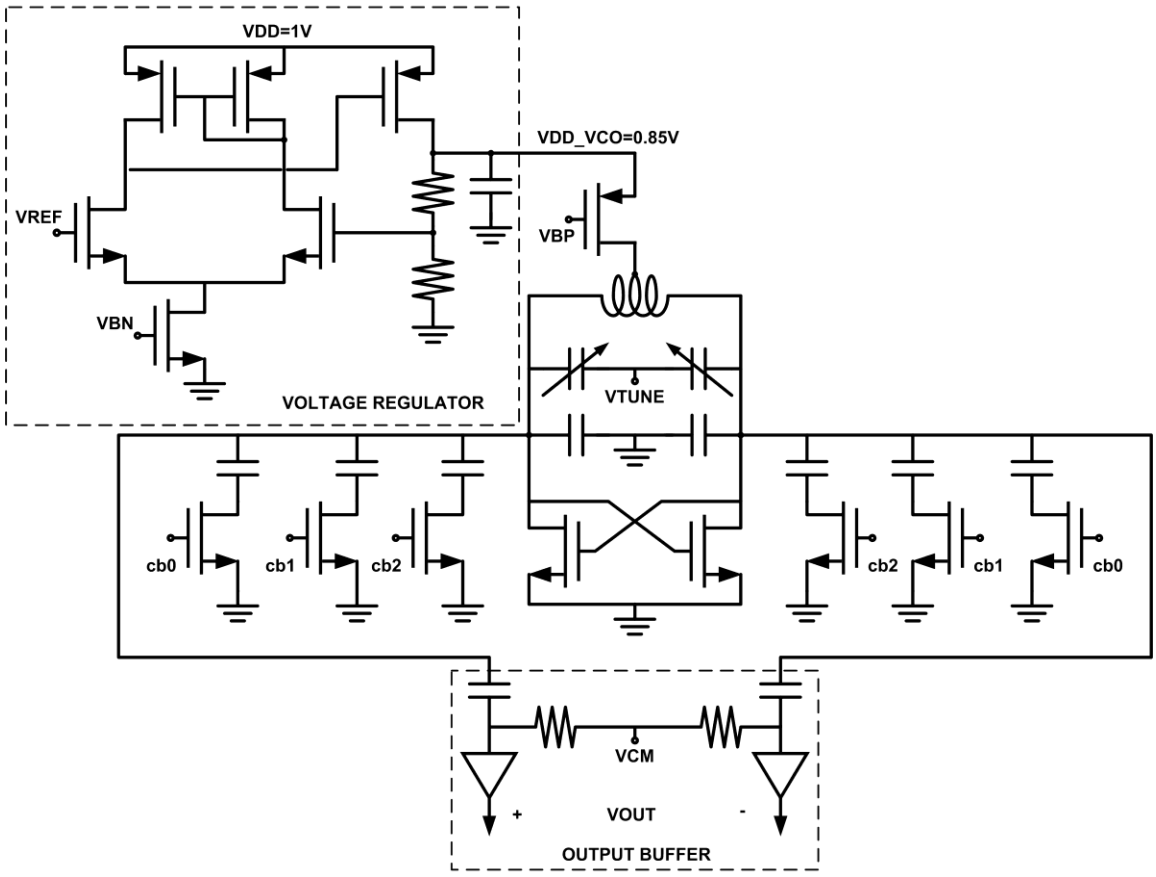
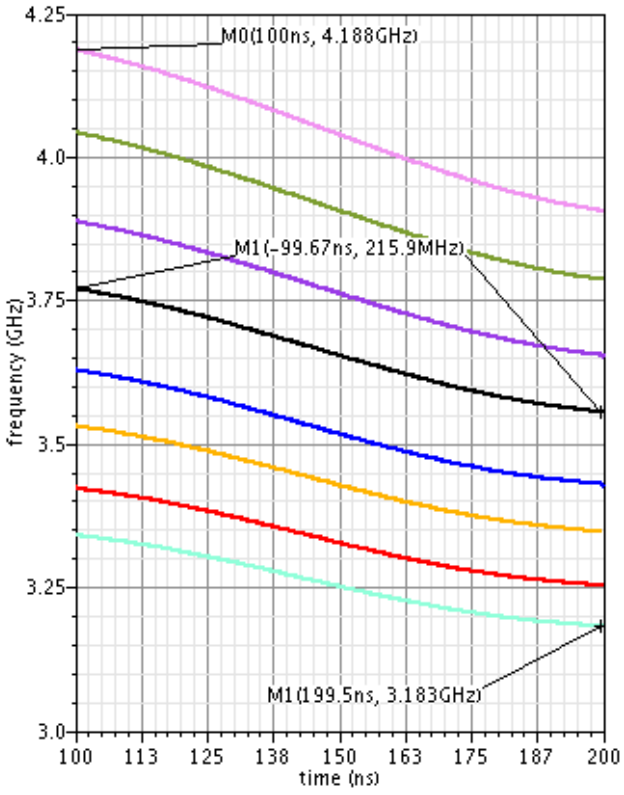
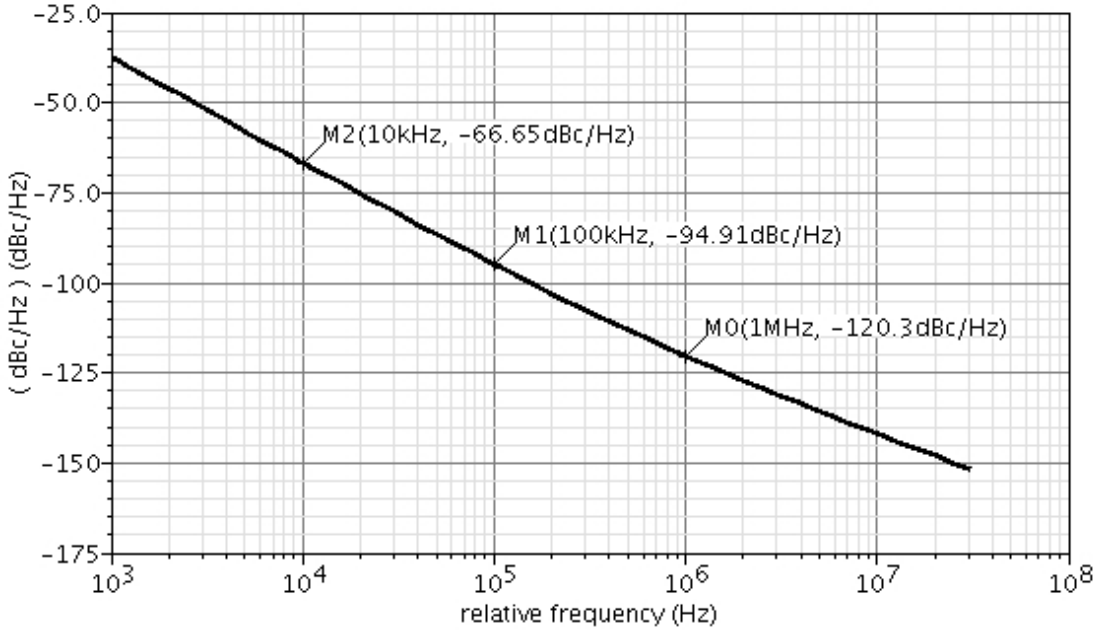


Figure 3.16. LC VCO schematic including the output buffer and voltage regulator.

The eight tuning curves obtained by varying the control word cb0-cb1-cb2 are reported in Figure 3.17(a). The K_{VCO} for each curve is about 220 MHz/V and total tuning range is 1 GHz. The power consumption for VCO is 8.9 mW. The phase noise for nominal condition including the voltage regulator is reported in Figure 3.17(b) for 3.456 GHz.



(a)



(b)

Figure 3.17. (a) VCO tuning curves for nominal PVT conditions. (b) Cross-coupled LC VCO phase noise for nominal conditions.

3.2.3 **Active Loop Filter**

To decrease the bandwidth of PLL, a large passive capacitor has to be used in a sigma-delta PLL. To decrease the area occupation while retaining a large capacitance value, the technique of capacitance multiplication is used. As shown in Figure 3.10, a nine-time current mode capacitor multiplier is adopted for a multiplication ratio of 10. The solution allows reduction on a passive capacitance by a factor of M. Compared with passive loop filter it can save M-1/M area. Main capacitance C_1 is implemented using MOSCAP capacitance to further reduce the area. There are two main design issues: working bandwidth and noise performances.

The schematic of the capacitor multiplier is shown in Figure 3.18. The multiplication factor is defined by the current mirror ratio. We can write the admittance Y_{in} as follows:

$$Y_{in} = \frac{I_{in}}{V_{in}} = \frac{I_{ox} + I_{p2} + I_i + (M-1)I_i}{V_{in}} = g_{ox} + sC_{p2} + M\frac{I_i}{V_{in}}, \qquad (13)$$

where g_{ox} is output transconductance of node X and I_i is the current flowing through main capacitance C_i.

Admittance Y_i can be expressed as

$$Y_i = \frac{I_i}{V_{in}} = sC_i//(sC_{p1} + g_{m1}) = sC_i\frac{1 + \frac{sC_{p1}}{g_{m1}}}{1 + \frac{s(C_i + C_{p1})}{g_{m1}}}, \qquad (14)$$

where g_{m1} is the transconductance of transistor M1. By integrating Equation (14) into Equation (13), Y_{in} can be expressed as

$$Y_{in} = g_{ox} + s(C_{p2} + M\frac{1 + s\frac{C_{p1}}{g_{m1}}}{1 + s\frac{C_i + C_{p1}}{g_{m1}}}), \tag{15}$$

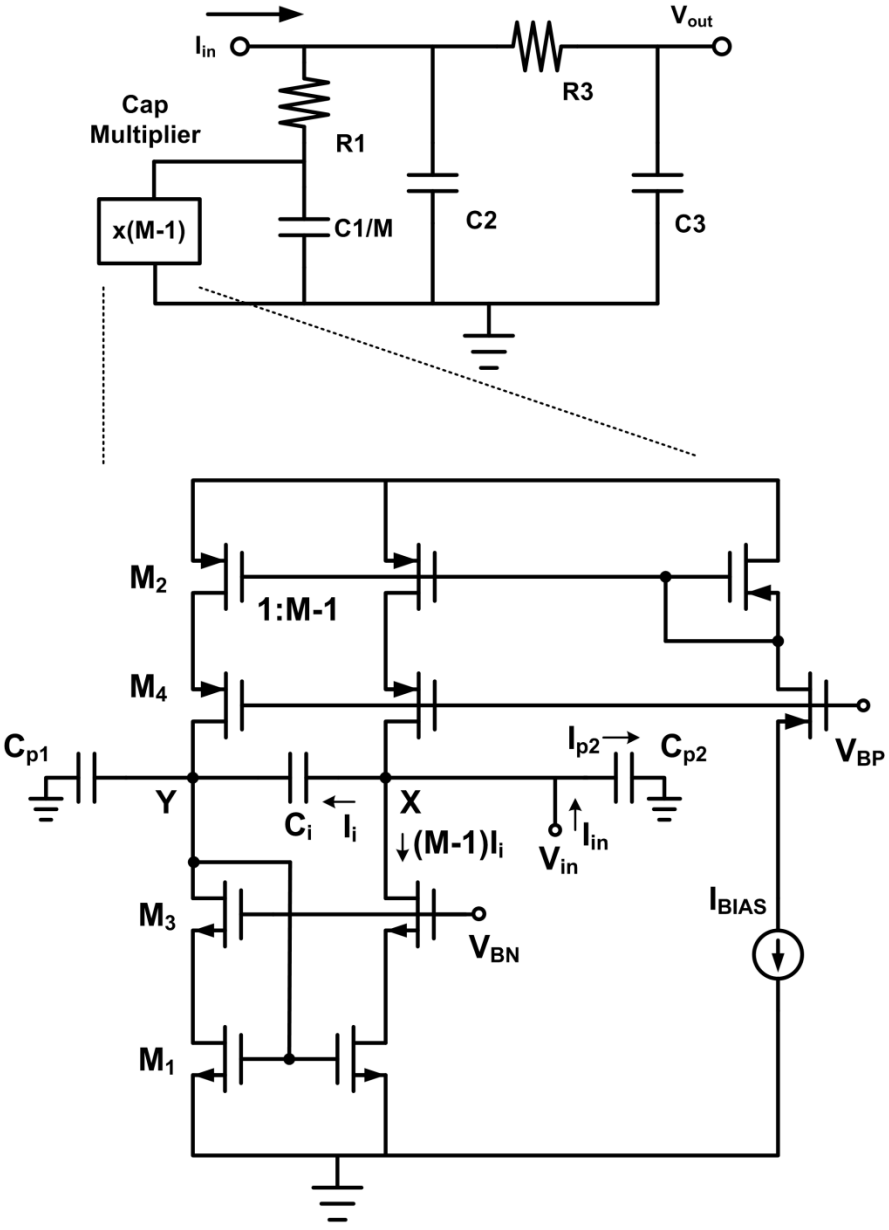


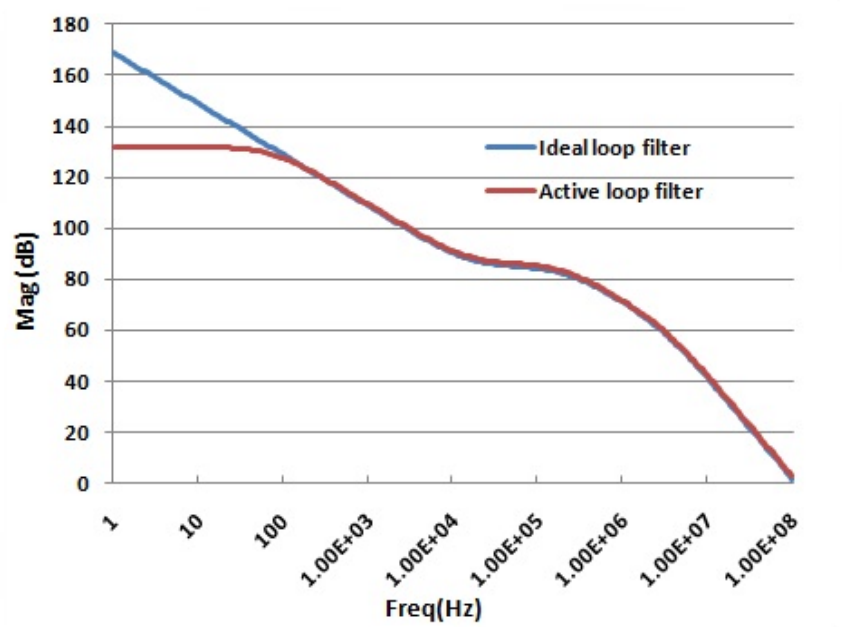
Figure 3.18. Current mode capacitor multiplier with cascaded structure.

There are one zero (gm1/Ci) and two poles (gox/(MCi) and gm1/Cp1) [20-22].The value of the current flowing through the circuit defines the position of the zero, which is the upper frequency limit. In order to maintain the phase margin, this zero frequency should be made much larger than the zero of the PLL. A cascoded structure is used to increase the DC output impedance that should be large enough to prevent current leakage from the charge pump. The output impedance value of active filter is set to about 120dB (1M Ohm).

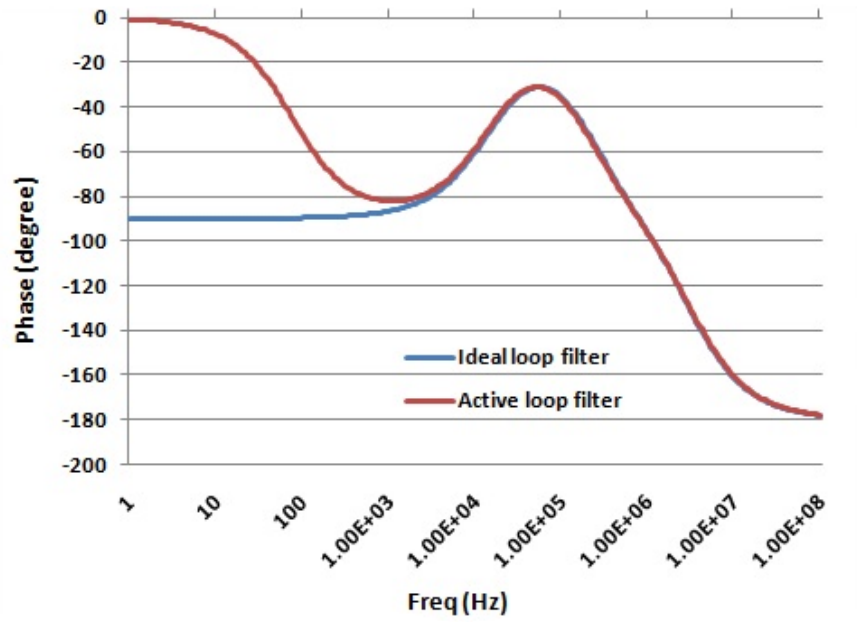
To have a better noise performance, we use long length devices and small current to decrease the thermal effect at 1MHz. The bias core is also considered and connected. On the other hand, the low frequency flicker noise contribution is a device characteristic and it is hard to eliminate.

Figure 3.19 is the AC simulation result of impedance and phase for the active filter, showing that the loop filter can be adequately operated for frequencies higher than 132 Hz. Different DC voltages at output of capacitor multiplier have also been tested, showing that a voltage range of 500mV is available (in the range 250-750 mV) with a DC impedance above 120 dB. Power consumptions for charge pump and active filter are 1.25 and 0.327 mW respectively.

The phase noise for PLL is concluded in Figure 3.20 from Matlab. By writing the transfer function to combine all noise contributions, the effects from active loop filter, charge pump, and sigma-delta modulator are shown. From the result, the phase noise changes from -120 dBc/Hz to -117 dBc/Hz at 1MHz offset, which is a good for system modulation.



(a)



(b)

Figure 3.19. The comparison of ideal and active filter: (a) AC response of impedance (b) AC response of phase. Red lines are related to ideal filter while blue lines are related to active filter. In this result, the active filter can be operated after the pole frequency 132 Hz. The DC impedance is about 135 dB.

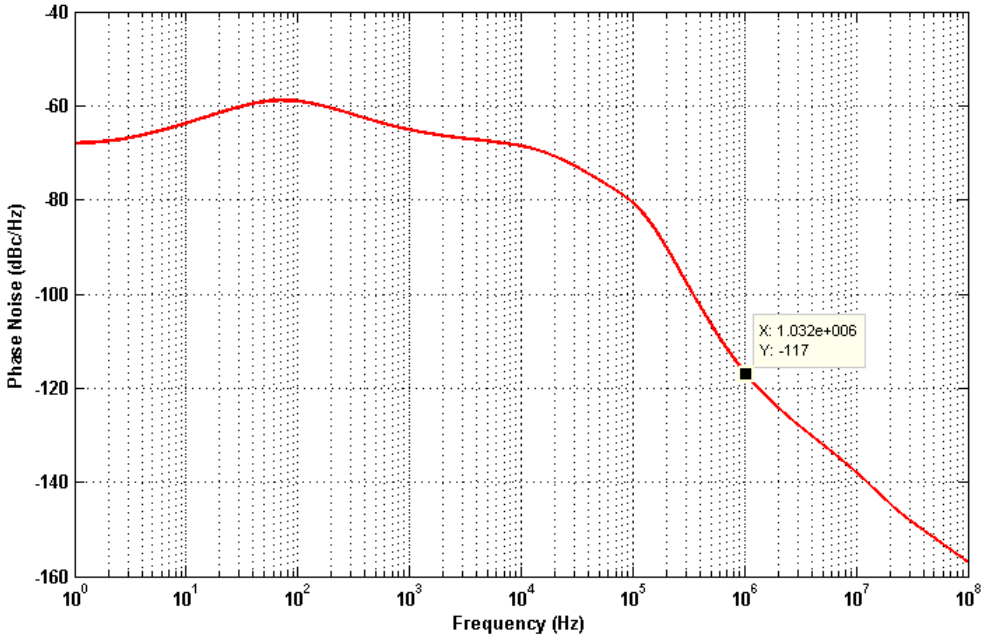
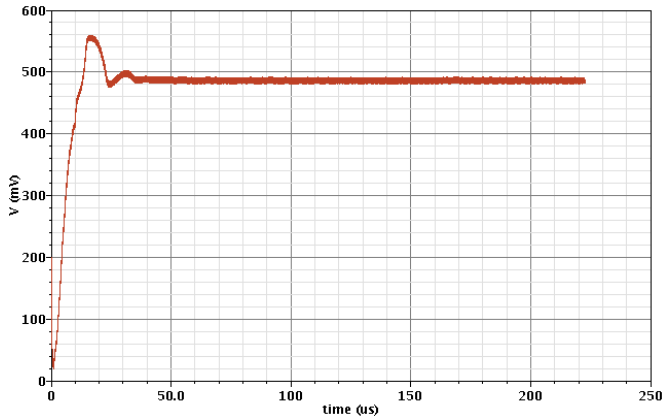


Figure 3.20. PLL output phase noise for active loop filter implementations.

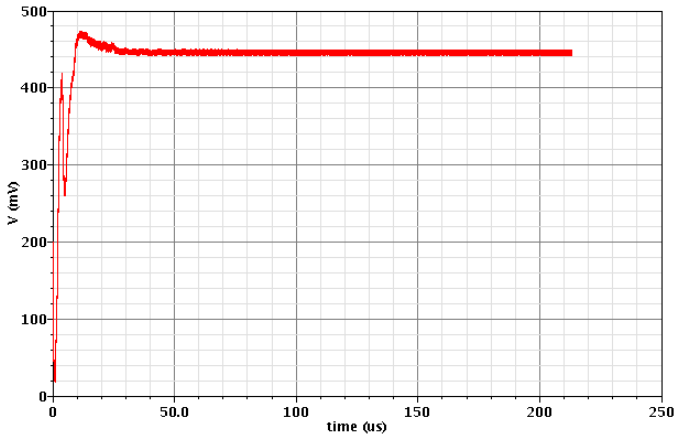
3.2.4 **Simulation Results**

The transient locking behaviors of the fractional PLL for 3.57 GHz with reference frequencies from 10 MHz to 40 MHz are shown in Figure 3.21. The simulation are run in Cadence using Verilog-AMS environment to include digital cells and transistor-level circuits in a PLL. As it can be seen, all settings are locked properly and the effect of the transistor capacitance dependence on the biasing condition is not impairing the loop stability. The layout of the sigma-delta PLL is shown in Figure 3.22. Total power consumption for this PLL is 12 mW.

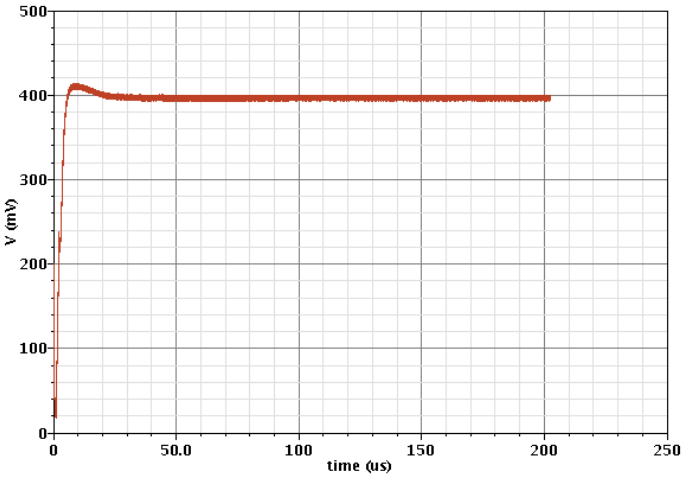
In summary, a 3.456GHz clock with a phase noise of -117 dBc/Hz (at 1MHZ offset) can be divided down to attain a phase noise better than -155 dBc/Hz (at 1MHZ offset) for 27 MHz.



(a)



(b)



(c)

Figure 3.21. The locking condition of the control voltage curve for 3.57 GHz with reference frequency equal to (a) 10 MHz (b) 26.49 MHz (c)39.44 MHz.

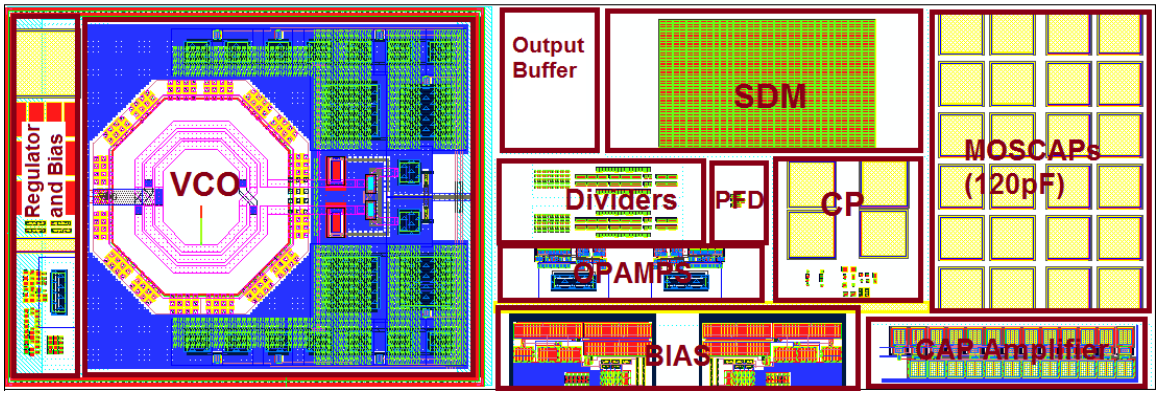


Figure 3.22. Layout of the sigma-delta fractional-N PLL (Area: 900 um x 300 um).

The performances of the baseband PLL is listed in Table 3.2 for comparison with the prior work in Table 2.2 targeting the similar frequency band.

Table 3.2. The baseband PLL simulation performances.

Spec. \ Ref.	This Work
Tech.	65nm CMOS
Freq. (GHz)	2.97-3.52
Tuning Range (%)	16.9
Supply (V)	1.2
Total Power (mW)	12
Phase Nose @1MHz (dBc/Hz)	-117
Area (mm^2)	0.27
Ref. (MHz)	10-40
FOM (dB)	176.4
FOM_T (dB)	181

*10 % FTR is used for FOM calculation
-Not provided in the paper

The FOM of VCO is expressed as

$$FoM(\Delta w) = L(\Delta w) - 20\log\frac{w_o}{\Delta w} + 10\,log\frac{P_{DC}}{1mW}, \quad (16)$$

where Δw is the offset frequency from carrier frequency w_o and P_{DC} is the static power of circuit in mill watt. An extended expression including frequency tuning range (FTR) for evaluation is

$$FoM_T = FoM - 20\log\frac{FTR}{10}. \quad (17)$$

The baseband frequency synthesizer achieve a good FOM_T with minimum power and area overhead, which saves a lot of cost that can be used for other system design and margin.

3.3 Frequency Synthesizer in RF

3.3.1 **Frequency Generation for Millimeter-wave Transceiver**

The proposed frequency synthesizer is implemented in a super-heterodyne transceiver as shown in Figure 3.23. This application targets mobile transmission in a short distance. Power and frequency coverage are important features for sustaining a long battery life and a wide bandwidth that is enough for the carrier to switch between the four channels on 60GHz spectrum. Instead of direct conversion, the RF PLL covers the channel frequencies on 48 GHz rather than 60 GHz, which provides more design margin on operating frequency. To further reduce the loading on frequency range, a 48GHz frequency doubler is used after the PLL. The actual requirement for the RF PLL becomes a bandwidth of 3.24 GHz on 24GHz RF. Moreover, there is no requirement for image rejection in the super-heterodyne transceiver compared with a direct conversion transceiver.

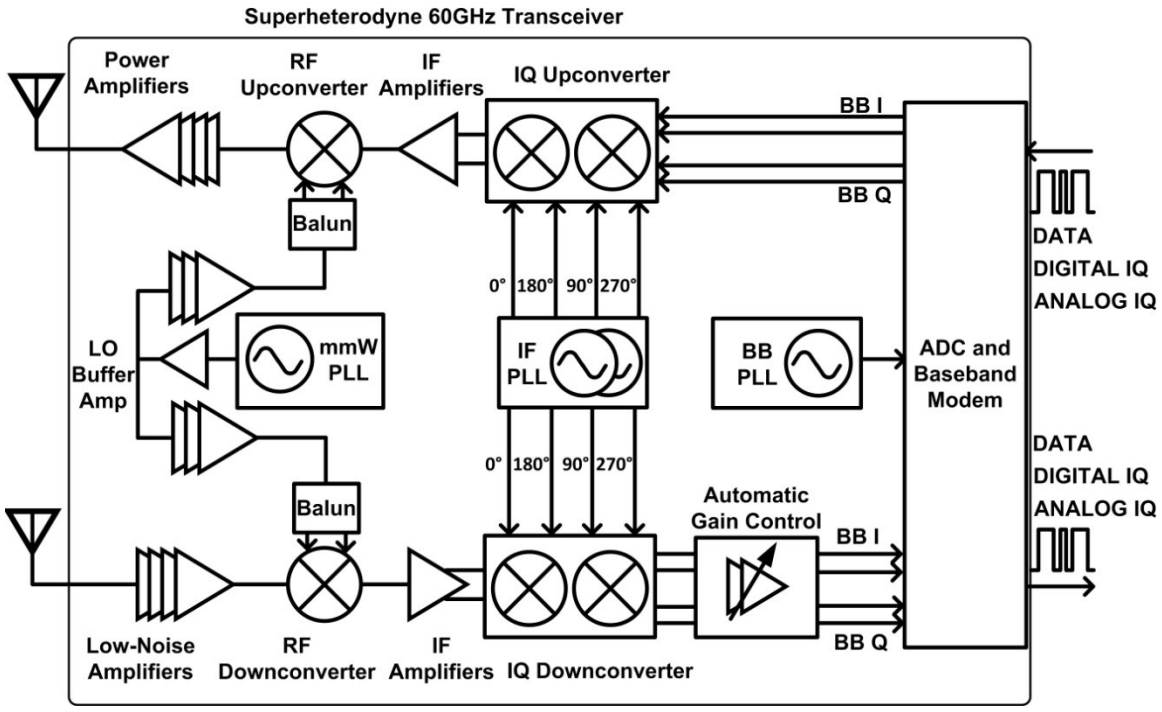


Figure 3.23. Example of the RF PLL in a superheterodyne 60GHz transceiver.

Figure 3.24 shows the proposed architecture of RF frequency synthesizer. The RF frequency synthesizer features an integer-N type 2 4th order PLL with dual-core double cross-coupled VCOs integrated with a programmable divider to cover the four channels with a phase noise less than -89dBc/Hz at the frequency offset of 1MHz. The frequency synthesizer outputs a 24GHz differential signal to a doubler, which delivers a 48GHz signal to TX and RX mixer using a power divider and 3-stage amplifiers. A regulator is designed on top of VCO to increase supply noise immunity and a lock detector is put in the divider chain to monitor the locking condition of PLL.

The lock detector is useful for the transceiver to react on the settling behavior of PLL as well. When the loop is locked, the back end circuits of transmitter and receiver starts to process the data. It is implemented by comparing the divided frequency with the input reference frequency in a digital manner. The low voltage low-dropout regulator

(LDO) provides a stable 1-V output as the supply of VCO. A high power supply rejection ratio (PSRR) is achieved. The PLL includes an adaptive charge pump and a reconfigurable loop filter as well. The adaptive loop dynamic provides more flexibility and margin for a high frequency PLL to adjust the acquisition speed and achieve a faster locking time. The technology node of CMOS 65nm is selected for implementation.

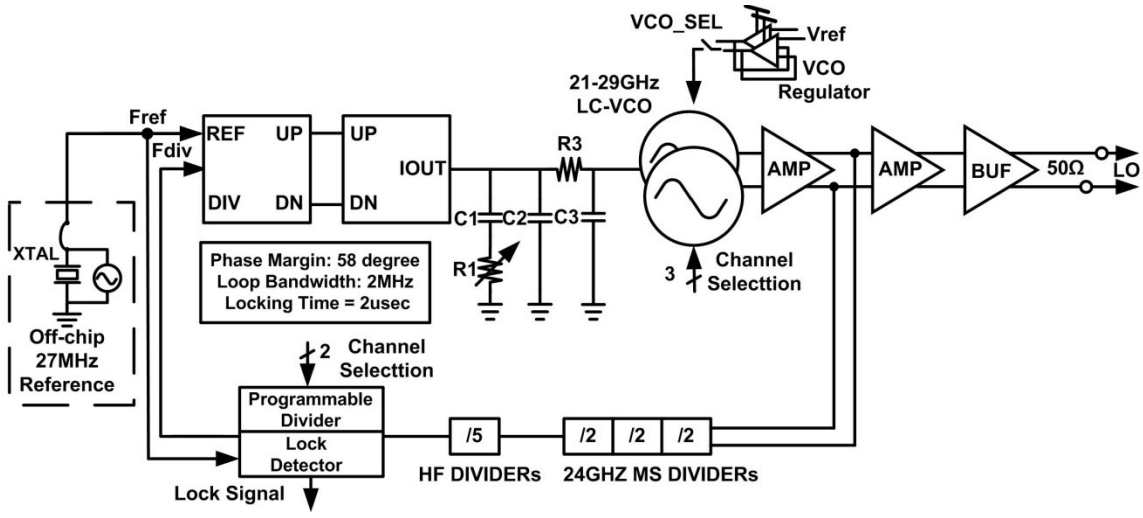


Figure 3.24. The integer-N RF PLL architecture to cover the 60 GHz operation.

3.3.2 **Building Blocks**

As shown in Figure 3.25, the double cross-coupled structure is selected as the core of VCO for better efficiency. This way, power consumption can be saved significantly for an integrated system. In order to cover a wide frequency tuning range, dual core VCOs are designed in the synthesizer. Each VCO are controlled by a three-bit input which results in eight tuning curves. Each curve is overlapped by adjacent curves for at least 60 % to provide continuous frequency shift in the VCO. The two VCOs overlaps one tuning curve with each other to prevent frequency shift between the two VCOs as well. Note that VCO frequency includes the effect from all varactors and

parasitic capacitances. Conventionally at a high frequency band, the circuit is sensitive to a small capacitance shift, and, therefore has a large K_{VCO}.

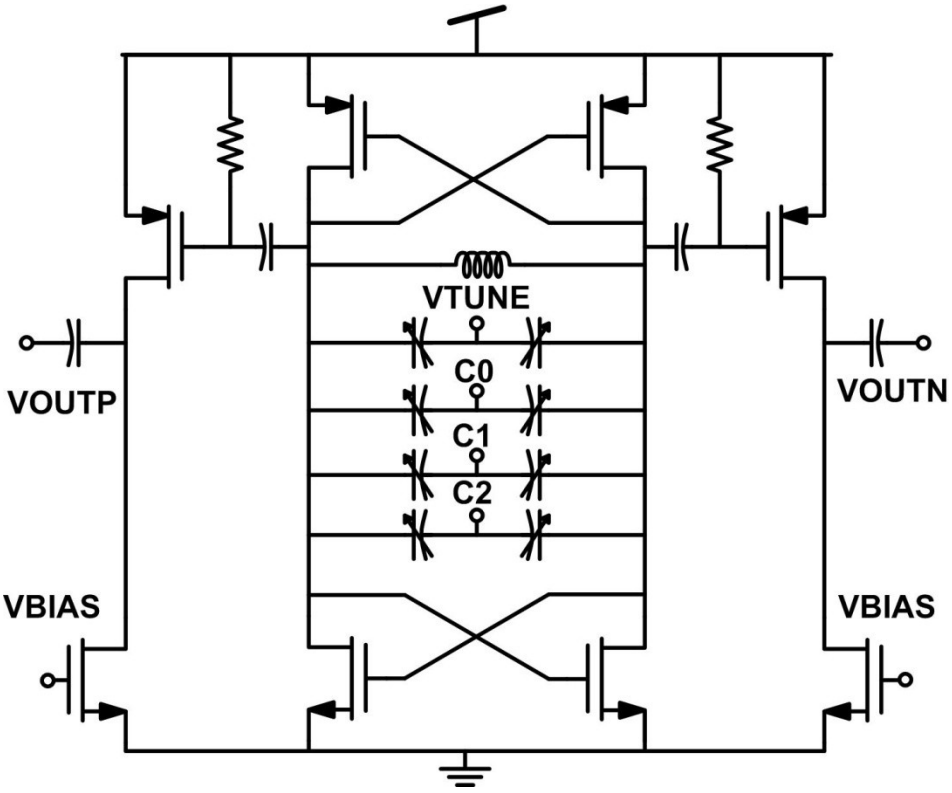


Figure 3.25. The diagram shows the schematic of single-core VCO using double cross-coupled structure for a low power consumption at 24 GHz. A three-bit control on the varactor provides programmability.

The prescaler is the first stage to divide the VCO output frequency down to lower frequency domain. Usually a small power can be achieved by digital circuits as well as the digital dividers. However, for high frequency operation logic gates are not reliable due to a small setup time and hold time. The feedback dividers are required to divide a 20GHz signal without any risk in this application. Current mode logics (CML) have to be adopted. In the process of 65nm, the trade-off is made at the frequency interface of 3 GHz. The three-stage prescaler is used to deliver 3 GHz frequency from 24GHz. Each stage uses the current-mode-logic (CML) architecture as shown in Figure 3.26. With constant current steering, the analog D flip-flop is able to be operated at high frequency

with wide range. Each stage is a divide-by-two circuit. The bias current increases with the operating frequency. Programmable bias circuits are also included in the PLL to provide enough current margin for the divider.

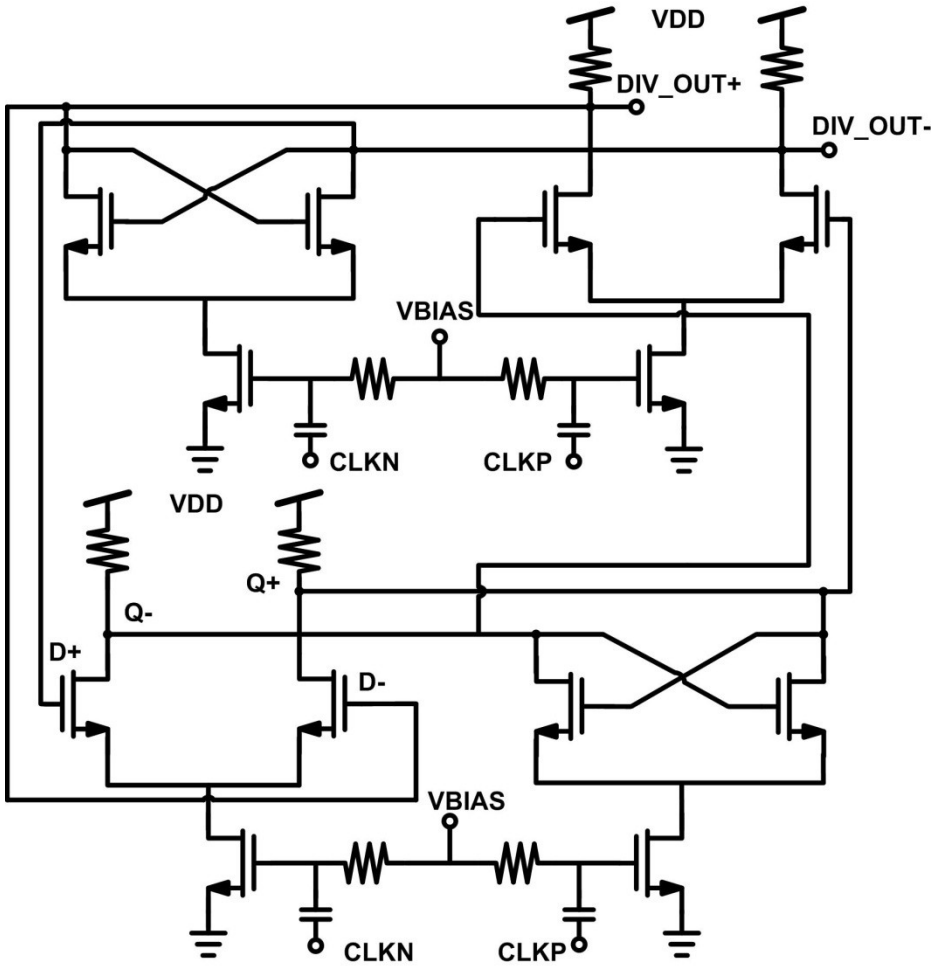
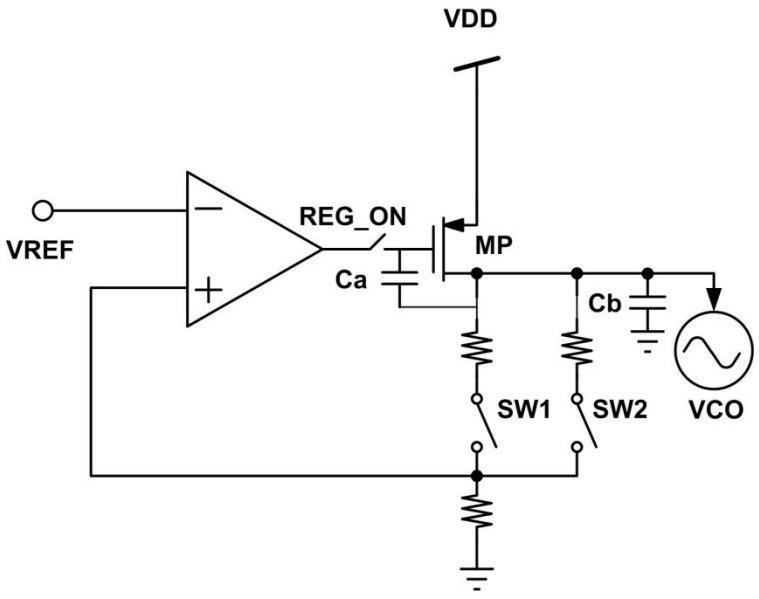


Figure 3.26. Schematic of the current-mode logic (CML) prescaler for high frequency division. Current bias is required to fix the current going through the circuit.

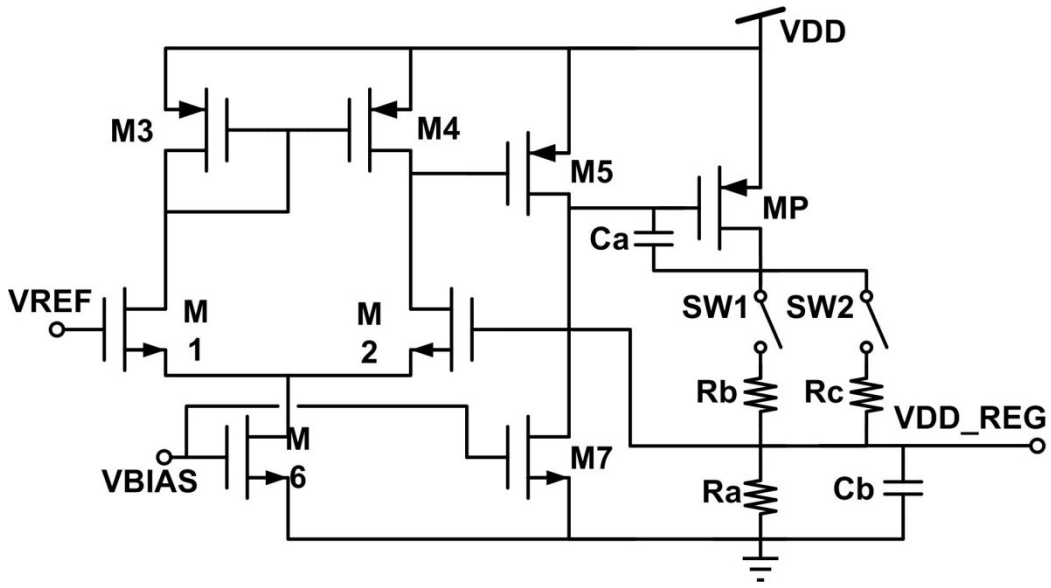
As shown in Figure 3.27(a), a regulator with 1-bit control is put on top of VCO to output two supply voltages from 1.2 V: 1 V and 0.9 V. The low-dropout regulator requires a high gain amplifier to regulate the output voltage. The PMOS transistor MP requires a large size to sustain the current drawn by VCO. In this design, The VCO

demands 12 mA. A PMOS transistor with 500 μm is large enough to provide the output current up to 40 mA.

In Figure 3.27(b), a two-stage amplifier is introduced to have a high gain and a wide bandwidth for the regulated supply. C_a is miller capacitance to make the dominant pole located at output of amplifier. There are total three poles in the regulator system. The current of the first stage of amplifier is designed to be larger than the amplifier output stage so that the pole is far away from that of the output stage. The third pole is the one at the PMOS output device, which concludes the output resistance and output decoupling capacitor C_b. The size of C_b would lead to a trade-off between regulator stability and supply decoupling effect. Larger capacitor would stabilize the ripples on regulated supply more efficiently with the risk of pushing the feedback loop into unstable condition. In the 24GHz VCO, a capacitor of 10pF is verified for the loop to have phase margin larger than 56 degree under all condition when current is varied from zero to 40 mA and output supply is varied from 0.9 V to 1 V.



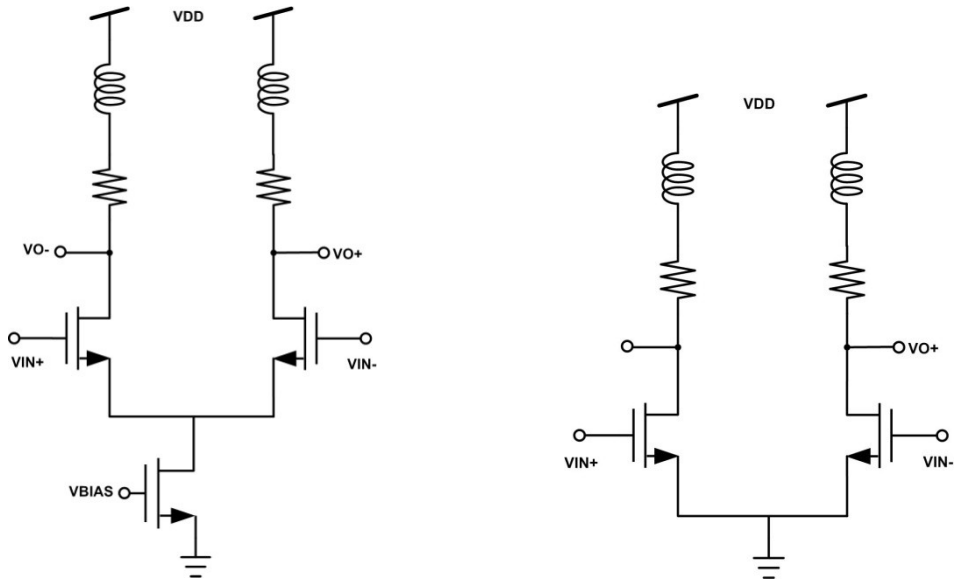
(a)



(b)

Figure 3.27. The circuit diagrams of (a) the LDO on top of the VCO and (b) details of the three-stage regulator with the supply switches to change the regulated voltage from 0.9 V to 1.0 V.

The output swing of VCO needs to be large enough to drive both divider path and output path. In order to compensate the loss along the signal path, two amplifiers and one output buffer as shown in Figure 3.28 are inserted in the PLL. The inductor is used for a wide bandwidth of more than 30 GHz, which covers the four channels occupancy on the spectrum. The current of amplifier is biased through a 2-bit control for a trimming on power, gain, and bandwidth. The output buffer is designed as a 50-Ohm interface for the purpose of measurement. It should be noted that the current of output buffer is affected by the common mode of previous stage. For a high gain cascaded stage it is risky to use a pseudo-differential structure since it may result a large input offset. However, at the RF PLL output, neither the gain of amplifiers is high nor the pseudo-differential input pair locates at the middle of the gain stage.



(a) (b)

Figure 3.28. The output amplifiers and buffer of RF PLL: (a) Differential inductor-peaking amplifiers and (b) Pseudo-differential 50-Ohm output buffer.

3.3.3 **Simulation Results**

The 1V 24GHz synthesizer is designed and extracted using TSMC CMOS 65nm technology. The total current consumption is 88.4 mA including the output buffer. There are eight frequency tuning curves due to the 3-bit control of varactor bank for each VCO. A total of 16 tuning curves are resulted to cover the bandwidth as shown in Figure 3.29 in this dual-core PLL design. Each of the 60GHz channel is covered by at least three curves. The current consumption of VCO and output source follower is 12.7 mA. The phase noise of dual-core VCO is shown in Figure 3.30 with the regulator configured to 1 V and the loop filter connected at the VCO input. The variation of K_{VCO} varies from 1.1 GHz/V to 1.8 GHz/V.

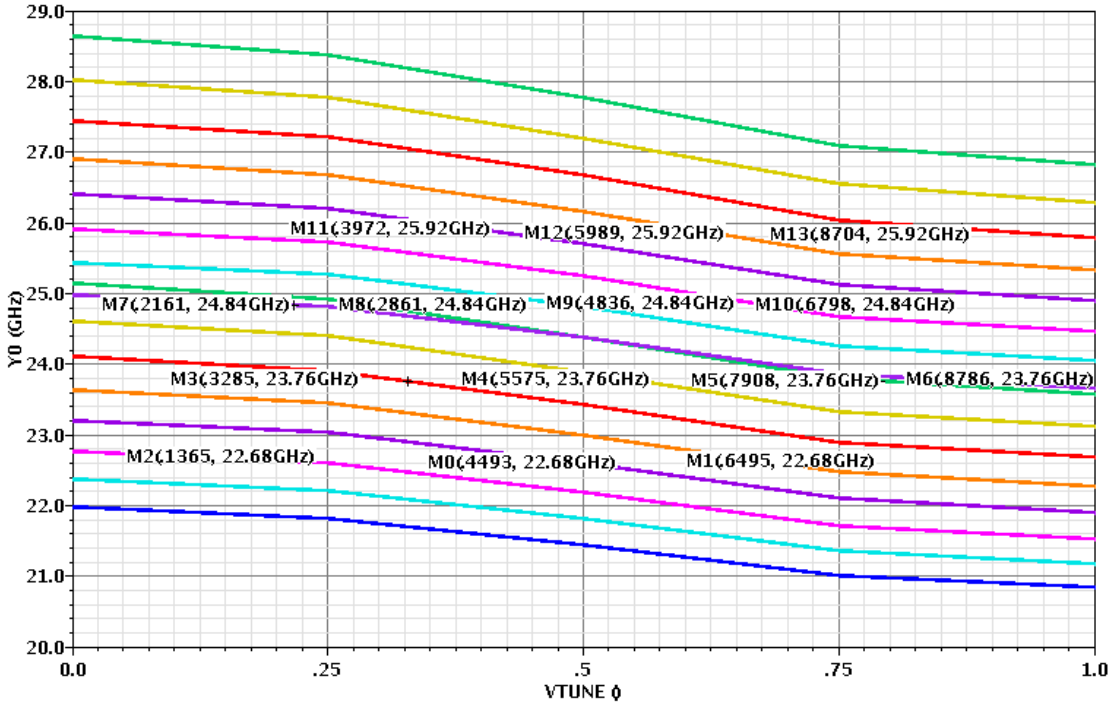


Figure 3.29. The 16 frequency tuning curves of dual-core VCO in RF PLL.

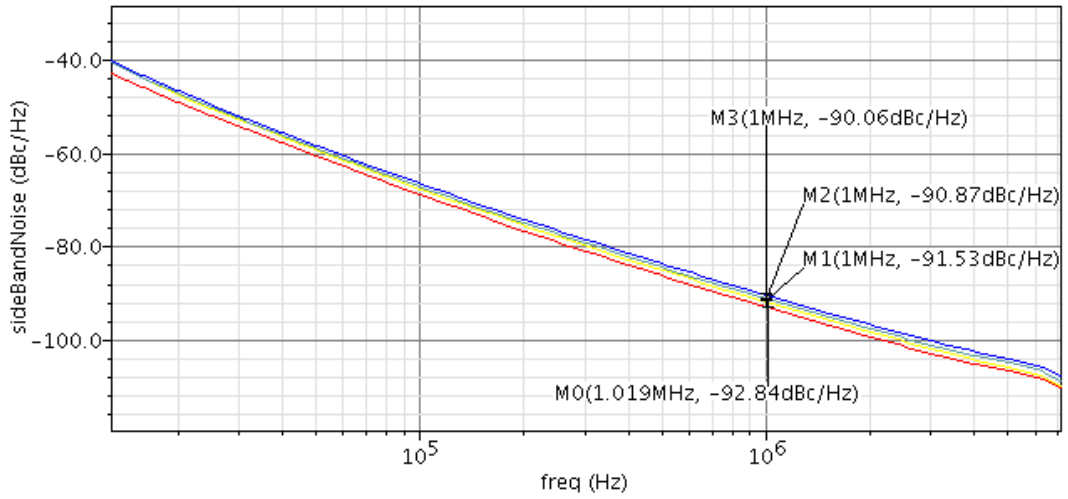
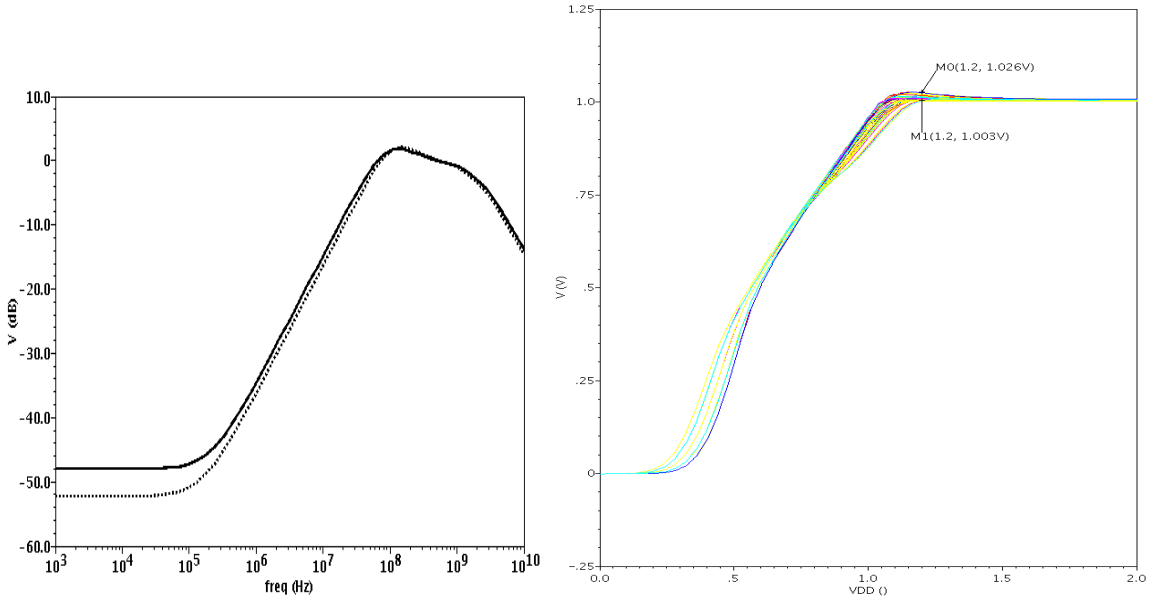


Figure 3.30. The phase noise of VCO outputs at four channel frequencies.

The regulator can be configured to support 1 V and 0.9 V. Figure 3.31(a) presents the PSRR of the LDO. The PSRR at low frequency is -48 dB for 1 V, and is -52 dB for 0.9 V. The 3-dB bandwidth is 200 KHz and a PSRR larger than -30 dB at 1 MHz. The

regulator has a loop gain of 53 dB and 57 dB when the output supply is 1 V and 0.9 V respectively. The current consumption is 550 µA.

Variation of output supply over different process corners using ocean script is performed to see the line regulation. The result is shown in Figure 3.31(b). A variation of 23 mV from 1.003 V to 1.026 V is obtained.



(a) (b)

Figure 3.31. (a) The PSRR and (b) line regulation of the regulator for the 24GHz PLL.

The RF PLL includes the sample architecture of charge pump and programmable loop filter in section 3.3.1 for adaptive loop bandwidth. The current of charge pump ranges from 190 uA to 1690 uA by programming the bias voltage.

Figure 3.32 shows The transition of the tuning voltage for the locking settings of the four channels frequencies: 22.68 GHz, 23.76 GHz, 24.84 GHz, and 25.92 GHz. A locking time of about 2 usec is achieved. Output spectrum after PLL is locked are put in Figure 3.33 for the four channels. Layout of the PLL circuits is placed in Figure 3.34.

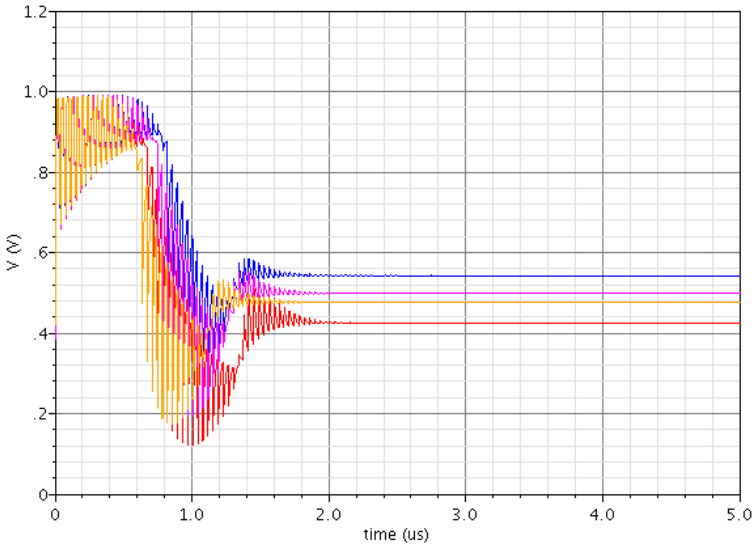


Figure 3.32. Locking waveforms of tuning voltages in RF PLL for four channels.

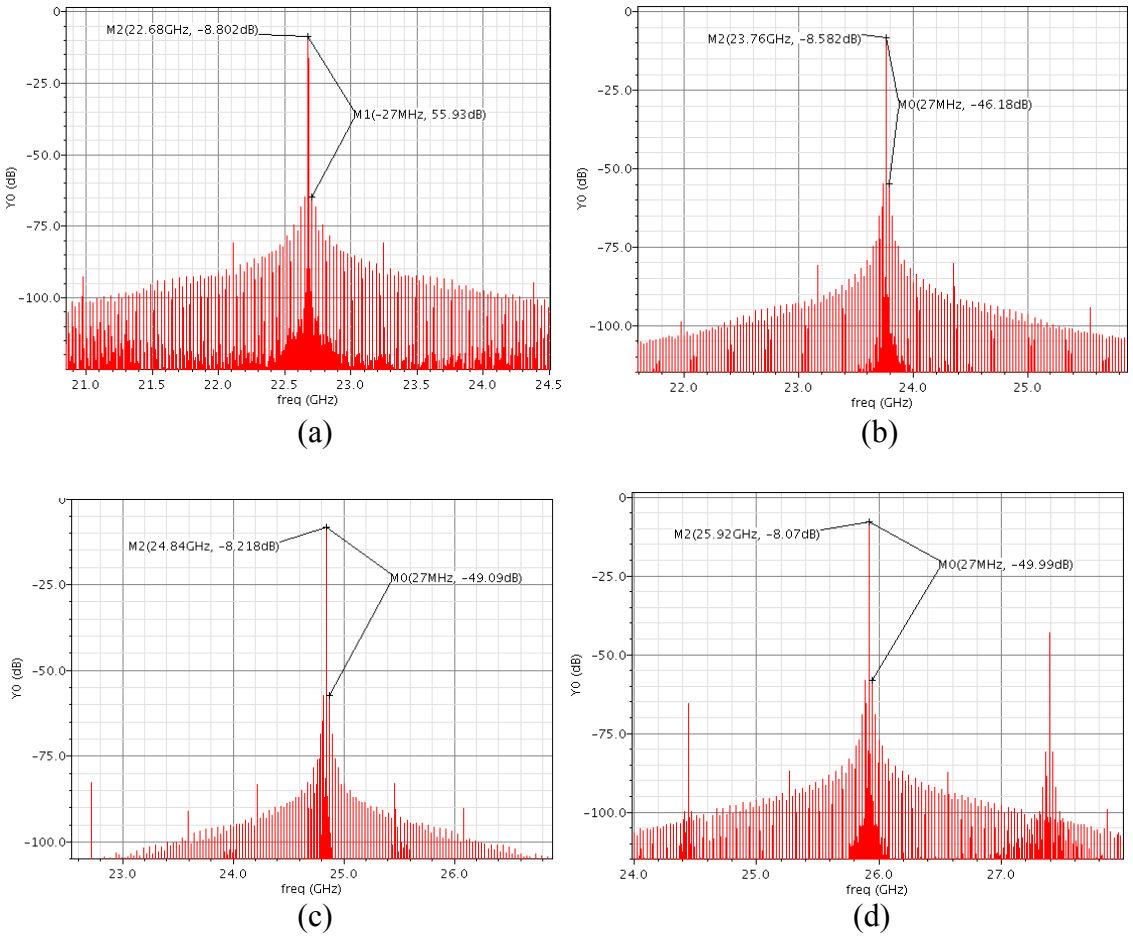


Figure 3.33. PLL output spectrums of four channel frequencies after the loop is locked: (a)22.68 GHz, (b) 23.76 GHz, (c) 24.84GHz, and (d) 25.92 GHz.

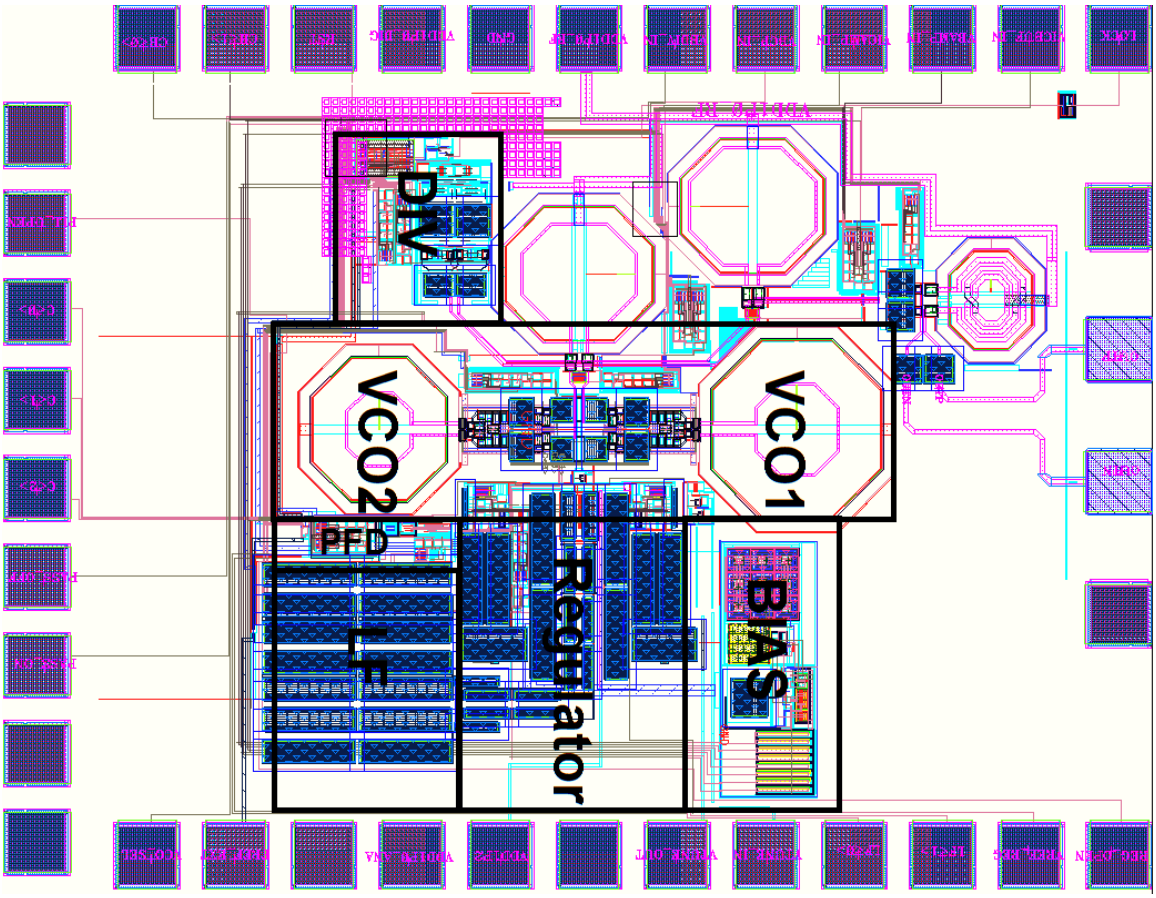


Figure 3.34. The layout of RF PLL. The area is 1150 um x 1000 um.

Table 3.3 is the summary of the RF PLL extraction result which concludes the extraction result from high and low band VCO. The PLL features a wide frequency coverage and a regulator for supply noise rejection. The figure of merit can be further extended to include the supply noise impact. The expression from Equation (17) can be written as

$$FoM_{ST} = FoM - 20\log\frac{FTR}{10} + \log PSRR, \tag{18}$$

where the PSRR is calculated in decimal value. The performance of this work is tabulated in Table 3.4 which shows a remarkable FOM_{ST}.

Table 3.3. The summary of RF PLL post-layout extraction.

Parameter		Post-sim	Unit
Supply Voltages		1.2 / 1.0	V
Current Consumption		88.36	mA
Locking time		1.5	uSec
Ref. Spur		< -45	dBc
Output Swing before first divider (Single-ended Vpp)	**H**	314	mv
	L	361	
Output Swing after output buffer (Single-ended Vpp)	**H**	422	mv
	L	463	
Phase Noise		-89.97 (25.64GHz)	dBc/Hz
H-band VCO Cover Frequency		23.75-28.64	GHz
L-band VCO Cover Frequency		20.84-25.15	GHz
KVCO		1.1-1.8	GHz/V
Dual Core VCOs Total Cover Frequency		20.84-28.64	GHz
Tuning Curve Overlap Percentage		>60	%

Table 3.4. The performance of this PLL is tabulated.

Ref. / **Spec.**	**This Work**
Tech.	65nm CMOS
Freq. (GHz)	20.84-28.64
Tuning Range (%)	31.5

Phase Noise@1MHz (dBc/Hz)	-90
Ref. Spur (dBc)	< -45
Reference Freq. (MHz)	27
Supply (V)	1.2, 1.0
Total Power (mW)	68^{+}
Area (mm^2)	1.15x1
PSRR (dB)	< -48
FOM (dB)	-159.6
FOM_{ST} (dB)	-172

[+]The current of output buffer is not included as other work
*Calculated assuming 20dB/decade degradation with offset frequency
-Not provided in the paper

3.4 Summary

This chapter presents the design of PLL with optimized performance and minimum overhead. A PLL with adaptable acquisition speed is first introduced for bandwidth and locking time control, which provides margin for high-speed application when a fast locking or a high bandwidth is required.

Secondly, a baseband 3.52/3.456/2.97GHz PLL is designed with an active loop filter for capacitance reduction. The PLL supports multi-gigabit communication in a 60GHz system with an area reduction of 90% in the loop filter.

Finally, a dual-core RF 24GHz PLL is designed to cover the wide bandwidth in mmW application. With the dual-core architecture, the PLL is able to be tuned from 20.84 GHz to 28.64 GHz. The frequency tuning range is 31% over the carrier frequency

of 24GHz. In addition, a voltage regulator is used to protect the noise-sensitive block from supply noise interference.

A complete verification process including post-layout simulation is performed for both baseband and RF PLL design. Comparison results with the prior art are provided to show the contribution as well.

CHAPTER 4: ANALOG-BASED SENSOR TESTING OF PLL

4.1 Introduction of PLL Testing Methodology

4.1.1 Conventional Testing and Limitations

Figure 4.1 shows the conventional setup for frequency synthesizer testing. The configuration allows users to monitor the performances closely by precise equipments including spectrum analyzer and digital oscilloscope. For a frequency synthesizer, the output is a clock scaled by a multiplication factor from the input clock. In order to verify the operation of CUT, frequency range, noise performance, and locking behavior are usually tested through the equipments attached to the output.

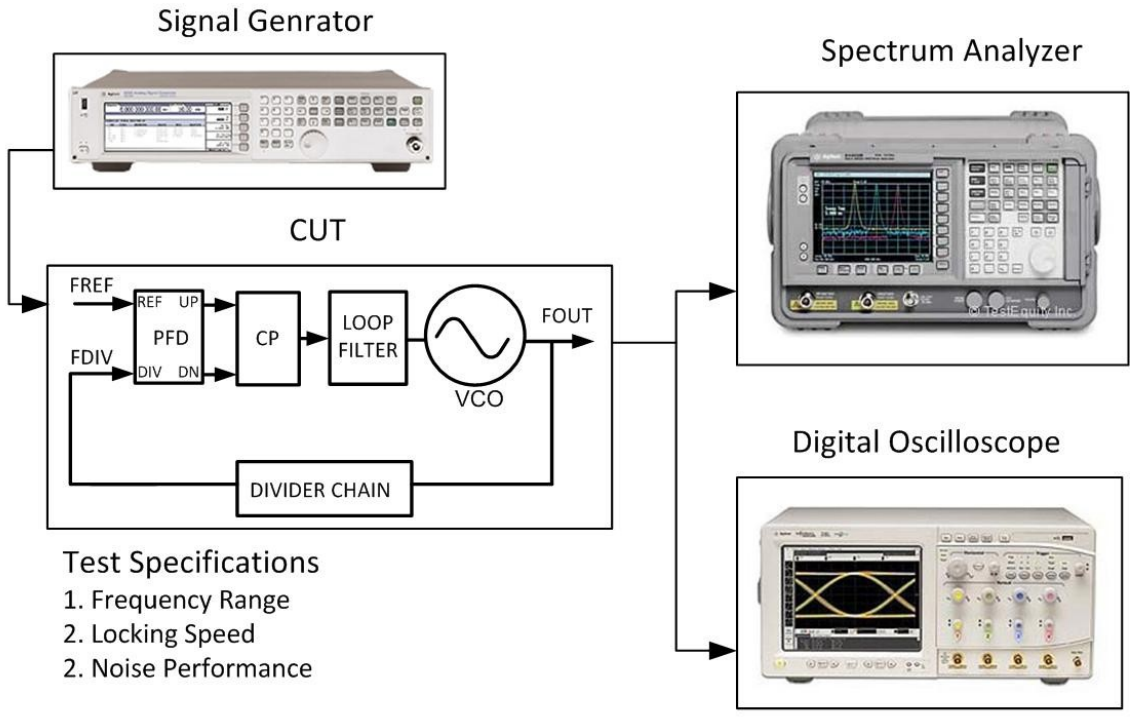


Figure 4.1. Conventional test setup for PLL.

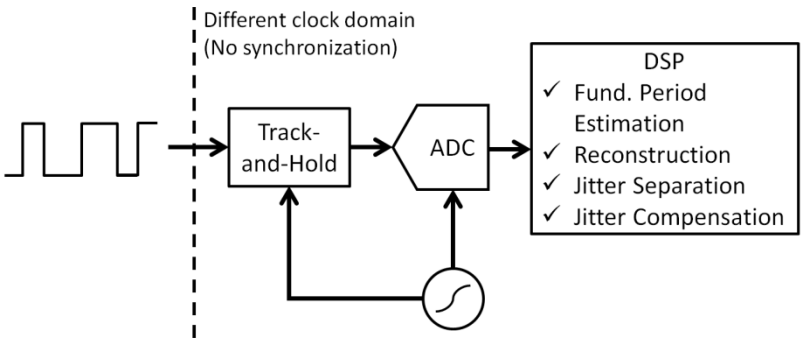
The locking range and noise performance can be easily tested through the spectrum analyzer and oscilloscope. However, it requires a continuous stimulus for production test. The process for test automation is complicated and expensive. The locking speed of a PLL can be approximated by observing the output spectrum through modulating its input reference signal with a slow clock. In this condition, the test flow to modulate the input reference and examine the output spectrum is even more costly than the frequency and noise test. Moreover, conventional PLL does not provide the access to internal nodes. The attempt to analyze the loop dynamic parameters is therefore difficult.

Different methodologies are available for PLL testing to save cost. Advanced digital signal processing (DSP) techniques are well-developed for high-precision testing today. Alternate testing provides a different mapping path for CUT parameters through adequate stimulus and response extraction. BIST is a direct solution to build circuits capable to test the performance on chip. These techniques are introduced in the following sections.

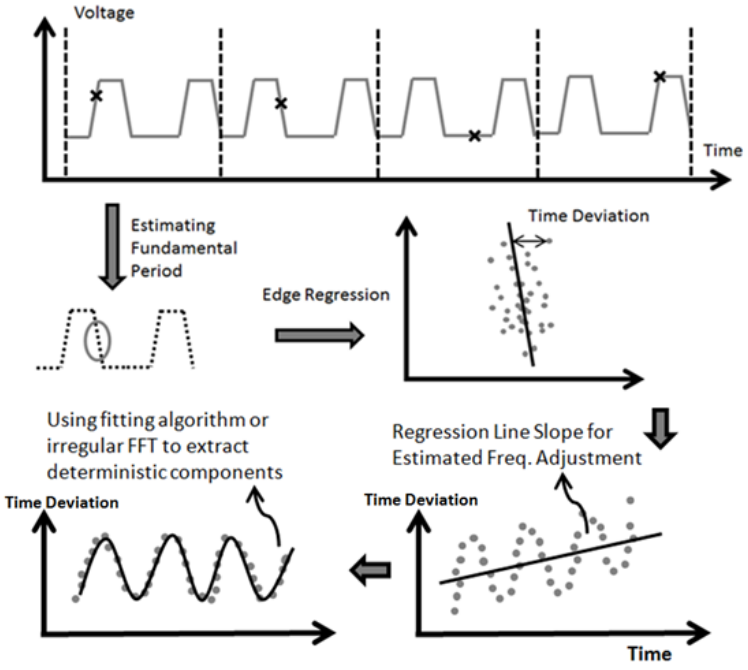
4.1.2 **Advanced DSP Technique**

Another methodology to save cost is applying DSP techniques for circuits testing. The conventional sampling theory to reconstruct a signal is to use Nyquist rate as the sampling frequency. However, it requires the front-end hardware at least two times faster than the CUT and hence increases the cost for testing equipments.

Instead an undersampling reconstruction can be used to greatly reduce the test hardware requirement [41]. Figure 4.2 shows the implementation hardware and reconstruction principle.



(a)



(b)

Figure 4.2. (a) The block diagram and (b) operation principle of incoherent undersampling reconstruction.

In incoherent undersampling reconstruction algorithm, periodic signal signals are reconstructed by minimizing the cost function [41] and estimating the fundamental frequency. Only the samples at the signal transition edges can provide information about the timing deviation of the samples. Using the samples at the transition edge, we can do fine frequency estimation and characterize the deterministic jitter component. Accurate

estimation is essential for high speed jitter measurement. Therefore, after coarsely estimate the frequency, fine adjustment is performed with the following equation

$$\Delta f = \frac{m}{1-m} f_{est} \tag{19}$$

where Δf is the frequency estimation mismatch and m is the slope of the regression line. As shown in Figure 4.2, to measure the timing deviation, we do linear regression for the samples at each transition edge, and the time difference between the samples and the regression line is the sample timing deviation, which contains the information of the periodic jitter and random jitter. The frequency of the periodic jitter usually is much lower comparing with the signal frequency. By plotting the timing deviation along the real sampling time, the periodic jitter can be characterized using a sinusoidal curve, and more precise information about the random jitter can be obtained by compensate periodic component using the fitted sinusoidal curve.

4.1.3 **Alternate Test Methodology**

Conventional test methodology for analog circuits is specification-driven. It means the circuit under test (CUT) is verified against its specifications. For example, an operational amplifier is characterized by slew rate, gain, bandwidth, and current capacity. A continuous stimulus and waveform monitoring for the production test is necessary. However, the process to measure the specifications of an analog circuit is complicated and the time to complete the process is long. Therefore, the alternate test methodology is proposed to reduce the time consumed for the production test [42-43]. This methodology injects a stimulus into the CUT and extracts the specification by characterizing the output response. A mapping function is applied to predict the specification parameters. As a result, the alternate test saves a lot of time in specification testing.

The alternate test can be realized as a mapping between various spaces. Figure 4.3 shows the mapping between the process parameter space (Ap), measurement data space (Am), and specification parameter space (As, performance space). Since circuit performances are affected by PVT variation, for any given device or semiconductor parameter combination in the normal operation region of process parameter space, a mapped result can be found in the measurement space. Similarly, a point in the specification parameter space can be mapped from the given process parameters. If the process parameter set is known, the specification can be easily calculated. However, it is not truth for the specification test. The other possible way is to build the mapping function between the measurement space and the specification parameters. The alternate test methodology directly predicts the specification parameters from measured data by establishing the correlation.

For alternate test, an appropriate stimulus and response extraction is significant for the construction of mapping function. The stimulus can be a DC or AC trigger signal to increase test sensitivity and cause optimal response. For example, a multi-tone signal is better than single-tone input for linearity test in CUT such as power amplifier (PA) and low noise amplifier (LNA). The stimulus-related response from CUT may need data converters and complicated analysis process. An efficient way to reduce the hardware overhead is to implement an on-chip sensor to convert the response to an easily interpreted response for the data acquisition and model establishment. In this chapter, the test of PLL will take advantage of an integrator as a response sensor.

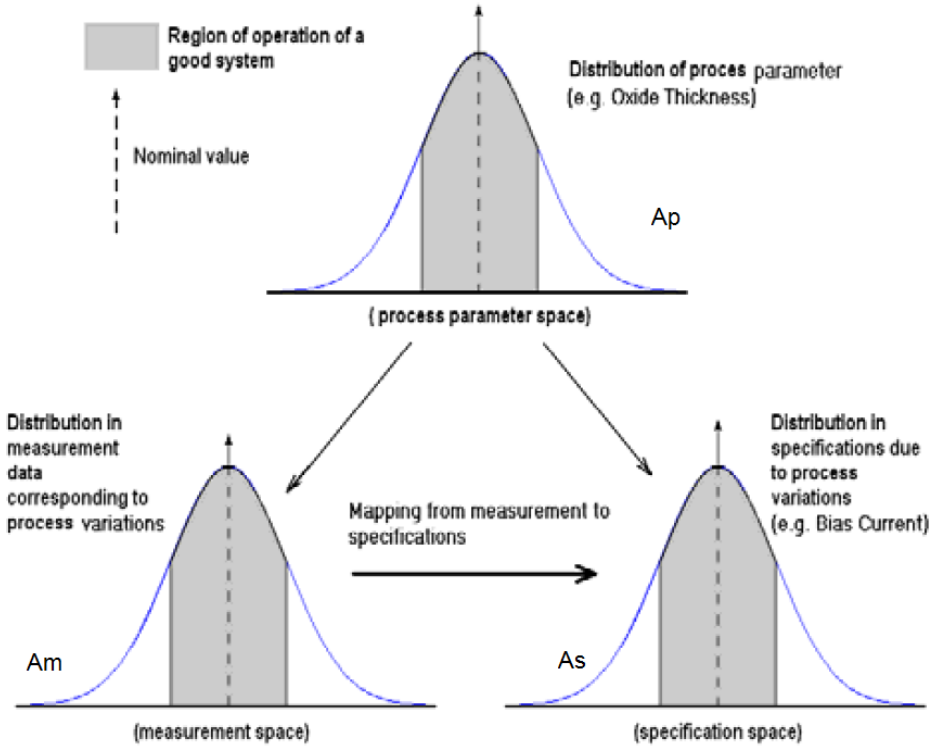


Figure 4.3. Mapping between the process parameter space, measurement data space, and specification parameter space.

4.2 Analog-based Sensor Testing for Loop Dynamics

4.2.1 Stimulus and Sensor Detection of PLL

In this section, we focus on measurement of the loop dynamics of a PLL, namely oscillator gain, charge pump performance, stability, and response time. There has been significant work on analysis and testing of PLLs, primarily for jitter [44-46]. The above specifications have an indirect impact on the noise performance (jitter) of PLL signals. For example, a jitter-free clock usually means that the VCO gain is small. Also, charge pump current mismatch leads to reference spurs in the spectral domain, which are a source of long-term jitter [47-48]. Further, PLL loop bandwidth determines response time and the speed with which a PLL can track the input clock. In a de-skew or spread spectrum application, high bandwidth is required in some cases for fast tracking

capability. Enough phase margin is essential for a PLL to operate across a wide range of conditions without losing stability. An unstable loop creates uncertainty in VCO frequency due to the damping behavior of the tuning voltage. Consequently, loop dynamics characterize different aspects of a PLL and have an indirect relation to PLL noise performance. Dynamic PLL performance parameters are also important for system-level performances of modern digital and mixed-signal SoCs.

The loop parameters in a PLL are important but seldom verified though external test interfaces. The open-loop transfer function of a PLL can be expressed by Equation (3). The charge pump and VCO are critical blocks of every PLL and are sensitive to process perturbations. An effective methodology for testing the loop parameters of a PLL after manufacturing is necessary for providing feedback to designers of integrated high-speed systems to improve device yield and for diagnostics.

In [35], a digital BIST is proposed for PLL loop parameter measurement. Loop gain, lock time, and lock range are the three main loop specifications that are tested. Digital frequency counters are used to measure VCO output frequency variation, and programmable delay circuits are used to adjust PLL input phase. Equations are derived for loop gain, frequency variation, and input phase offset. Lock time is measured by interrupting the loop and counting the number of reference cycles until the input phases are re-aligned. Lock range is estimated in an open loop test configuration from VCO output frequency. These methods require the use of digital circuitry and backend calculations.

This section proposes a simple test method that allows multiple PLL performance parameters to be extracted from a single test application. The DC values obtained from a

suite of sensors designed into the PLL loop are used to extract the relevant PLL dynamic loop parameters. This significantly reduces the complexity of the BIST infrastructure.

A block diagram of the PLL, reset MUX, and response detection circuits is shown in Figure 4.4. An analog MUX is inserted at the input of VCO to unlock the entire loop. The trigger signal also initiates sensor based response evaluation. The MUX does not affect the loop because the tuning voltage is bypassed to the oscillator and the MUX serves as a small parasitic capacitance when there is no reset signal. When the reset signal is pulsed, the tuning voltage node is discharged and the sensors are triggered. Detection and analysis starts at the same time with the P-type and N-type switch-based integrators functioning as PLL response sensors.

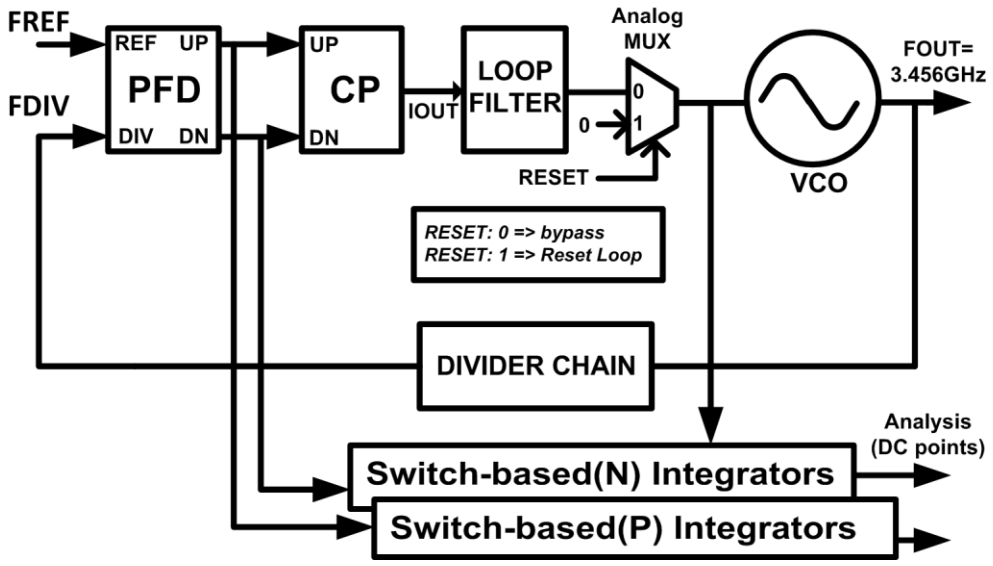


Figure 4.4. The analog multiplexer of PLL introduces reset signal in the loop to trigger the integrators as behavior sensors.

Two signal interfaces in the loop are selected for insertion of test circuitry. One interface is the tuning voltage connection between the charge pump and the VCO. The charge pump directly stimulates this node and modulates the VCO. The effect of the loop

response on the voltage waveform at the VCO control input due to the applied excitation is correlated to the stability, phase margin and locking time of the PLL.

The other interface consists of the outputs of the phase frequency divider that drive the UP and DN control signals of the charge pump. The UP and DN signals determine when the VCO tuning voltage node is charged (to increase VCO frequency) or discharged (to decrease VCO frequency). For a VCO with high gain, the phase offset at the PFD is small because the VCO sensitivity to changes in its control voltage is high. The bandwidth and settling time of the PLL are correlated with this phase variation at the PFD over time as well. Consequently, phase variation over time can be used to analyze the loop dynamic parameters as well.

If the reset signal is not asserted, the system remains in its phase-locked state. When the reset signal is asserted, the operation of the PLL is interrupted by the injected disturbance causing it to go out of its locked state. Consequently, in the absence of the trigger signal, the loop starts tracking the reference signal until lock is again established at a future point in time. Monitoring of three input response signals including the UP, DN and VCO control (tuning) voltage is performed through the duration of time until PLL phase/frequency lock is established again. A total of six DC voltages are acquired from six integrators for PLL loop parameter tracking.

4.2.2 **Sensor Design**

The schematic of P/N-type integrators and analog MUX is shown in Figure 4.5. The input voltage is accumulated at the integrator output. Since the N-type integrator is ground referenced, it is sensitive to high voltage variation while the P-type is relatively sensitive to low voltage variation with supply as a reference. When the input transistor is

active, it operates as a switch to induce current and charge on the output node. In order to shut off the current, an enable transistor is cascoded between the integrator and the rail voltage. When the PLL is reset, ground and supply referenced integration starts with the two types of integrators enabled.

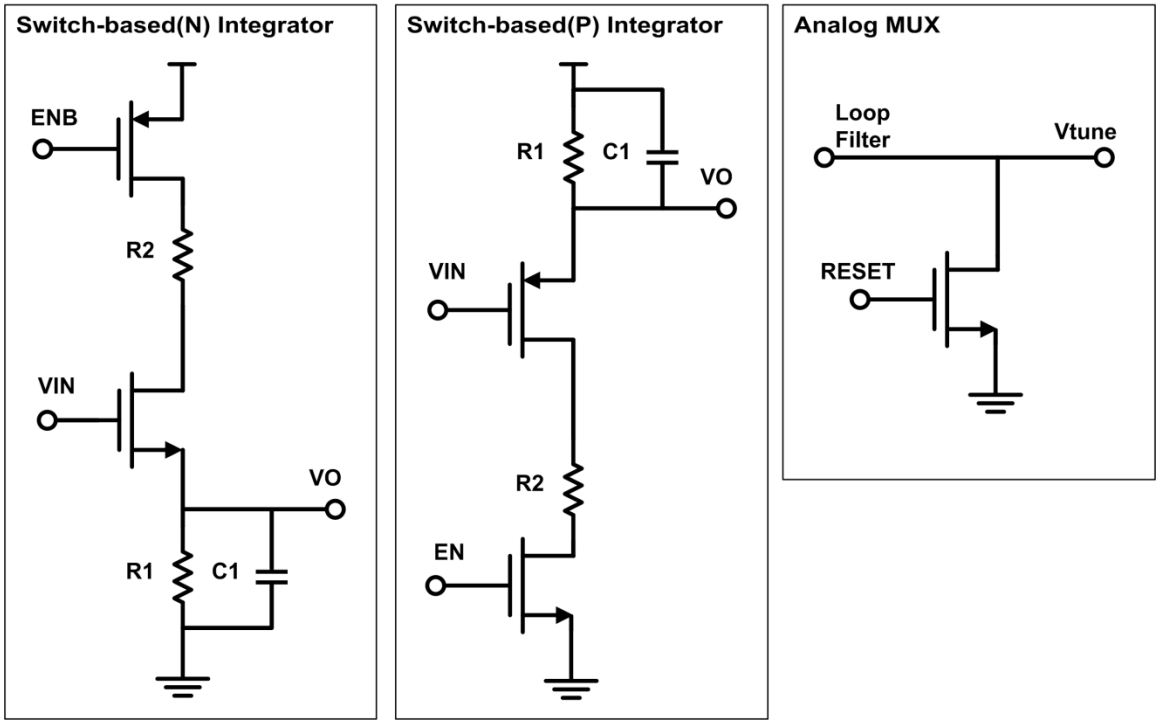


Figure 4.5. Proposed design of integrator and analog MUX for PLL loop parameters detection.

An analog multiplexer is placed between the loop filter and the input of the VCO so that it can bypass the controlling voltage in default operation. The MUX is implemented by a simple NMOS transistor. When the input voltage is low, the device is turned off. The loop filter impedance remains the same as the device only serves as a small parasitic capacitor. When the MUX is active, the loop is unlocked with the connecting node discharged to ground. In order to reduce the leakage current and loading effect on the PLL, a small thick-oxide transistor is used.

The transient response waveforms of PLL and integrators outputs to reset signal are shown in Figure 4.6. From 0 usec to 10 usec, the loop is locked and remains unchanged until the reset pulse is activated. The analog MUX in Figure 4.5 immediately resets the tuning voltage and then initiates a new locking transition, which produces new data for the integrators. When the loop approaches the phase-locked condition, the integration also concludes concurrently for a DC value.

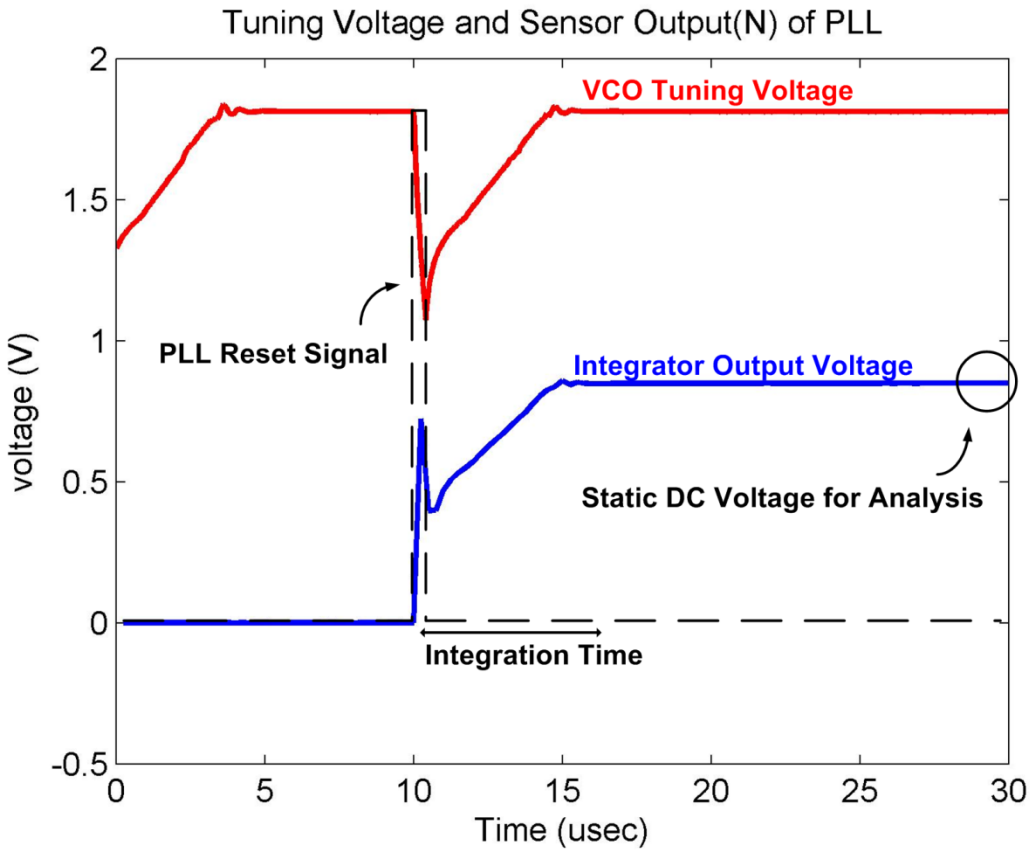


Figure 4.6. PLL loop responses to a reset signal in the loop. A relocking happens after the reset signal is diminished. The integrator output also starts working. Only a DC voltage at the end is required for analysis.

Since there is no fluctuation on the tuning voltage at the static state the integrators outputs will finally converges and provide static voltages. The static DC point is sampled

as the evaluation signature. To avoid additional current consumption the integrator is turned off at the end of response evaluation.

4.2.3 **Loop Performances over PVT**

A 3rd order integer PLL is designed in CMOS 0.18um process with a frequency locking range from 2 GHz to 5 GHz. The VCO core is utilized by a ring oscillator with the supply voltage as a proportional path for output frequency tuning. The proportional path current is steered by a PMOS current source, which is controlled by the charge pump and connected to the loop filter as an integral path.

The robustness of frequency dividers is necessary to overcome all PVT conditions. The feedback dividers are composed of current-mode logic (CML) and digital blocks to operate at the target range with margin. At a frequency of 5 GHz, digital gates in this process will lose reliably in extreme corners. CML dividers are used to fulfill the high frequency requirement. For frequency divider design, a trade-off exists between the power consumption and reliability.

A tri-state phase frequency detector is implemented in order to differentiate the rising/falling edges of reference and divided clock. Charge pump current is programmable for control of different loop gain. A dynamic current range from one to four is available to vary the bandwidth of PLL.

The summary of PLL loop performance is listed in Table 4.1. To validate the response evaluation, complete simulations are performed over process, voltage, and temperature corners. Reset of PLL and detection of integrators are applied for a total of 255 cases with the output being locked at 3.456 GHz. Moreover, the area and power budget of PLL including all six integrators are calculated in the table. The power

consumption and the area utilization of sensors is about 11 % and 2 % of the PLL core respectively. An on-chip testing solution is achieved with a relatively small overhead.

Table 4.1. PLL loop performances summary.

Specification	Tested PLL (Applicable Range)
Process Node	CMOS 180nm
Output Freq. (GHz)	3.456 (2 - 5)
Reference Freq. (MHz)	48 (10 - 50)
Division Ratio	72 (16 -128)
DC Power (mW)	8.4 (3.6 - 11)
Charge Pump Current (uA)	20 (10 - 40)
Supply (V)	2.5/1.2
Bandwidth (MHz)	3 - 6
Locking Time (usec)	4 - 12
Charge Pump Current (uA)	20
PLL Area Estimation (mm^2)	0.16
Total Sensors Area Estimation (mm^2)	0.003387
Total Sensors Power (mW)	0.93
Process Corners	ss, tt, ff
Temperature (degree)	-40,-30, -20, ...90, 100, 110, 125
Supply Variation (%)	-10, -5, 0, +5, +10

4.2.4 Simulations and Experiments

Different process and parameter combination leads to different circuit performances. For oscillator, the free-running frequency becomes lower in corners including low temperature and slow process where the small mobility of device results in a small gain and a narrow operation bandwidth. At high temperature and fast process corners the device operates vice versa. In this proposed method, specifications under

different environment factors are recorded as a parameter set for the following evaluation process.

Gain of VCO features the frequency variability over an specified input range, and is usually noted at KVCO. The integral and proportional gains of VCO are simulated as shown in Figure 4.7 for this design. Over PVT the variation of integral path gain is found to be two times larger than the minimum value, while that of proportional gain is from 3 GHz/V to 5.4 GHz/V. The histograms of gains are shown in the figure. The prediction is therefore critical to cover a wide variation.

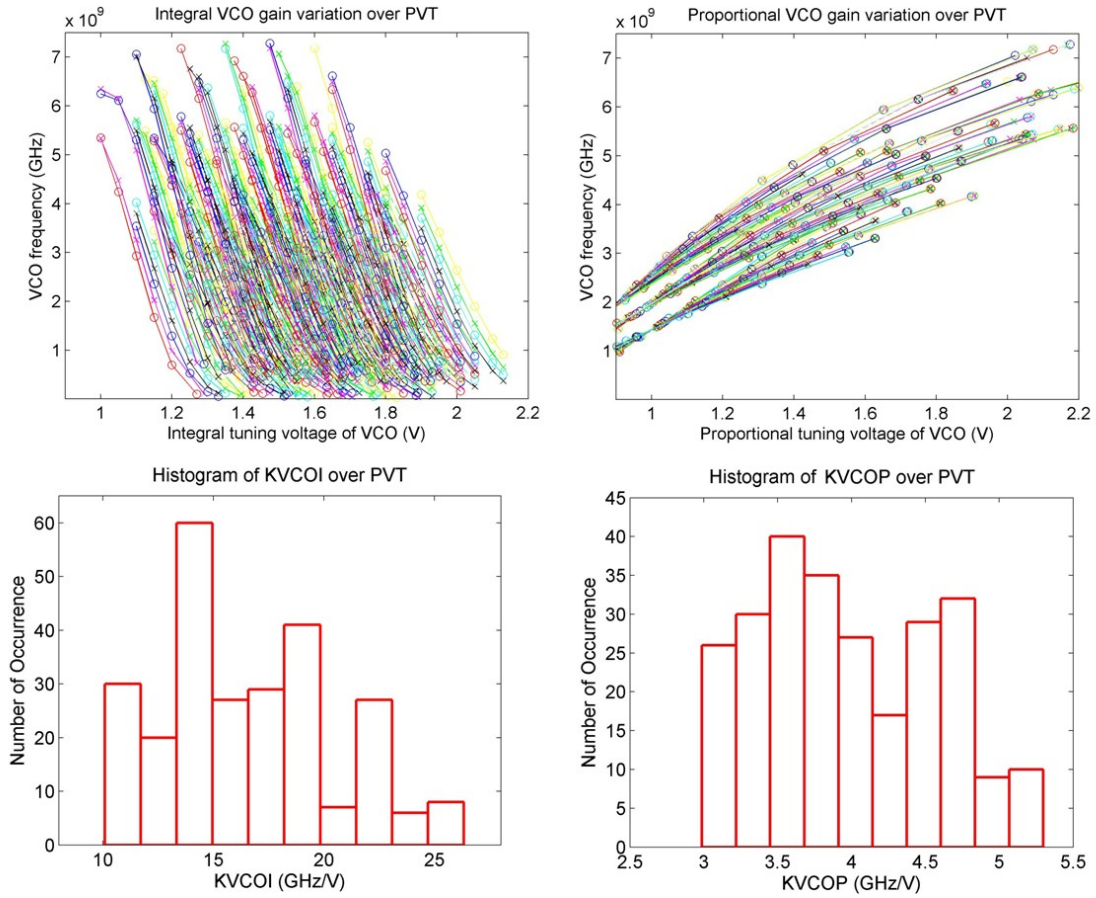


Figure 4.7. The transfer curves of VCO integral and proportional gain in the PLL. The results are simulated over 255 PVT corners. Histogram of gain values are attached at the bottom of the transferring curves.

Locking time is measured after the reset signal is applied and determined by the loop bandwidth. Charge pump current is calculated based on the average of charging and discharging current. Bandwidth and phase margin are resulted from the PLL loop equation (3) where reference frequency, division ratio, VCO gain, and charge pump current are known specifications over PVT. The statistic number of the six target specifications is listed in Table 4.2.

Table 4.2. Statistic data of parameters to be predicted.

I_{CP} (uA)	Mean	19.5024
	Std. deviation	5.5963
K_{VCOI} (GHz/V)	Mean	16.5564
	Std. deviation	3.9634
K_{VCOP} (GHz/V)	Mean	3.9765
	Std. deviation	0.5897
Locking Time (usec)	Mean	6.2686
	Std. deviation	1.3721
Bandwidth (MHz)	Mean	4.3412
	Std. deviation	0.76
Phase Margin (^{o})	Mean	52.9791
	Std. deviation	1.8454

The tuning voltages and one of the integrator output waveforms over all the corners are shown in Figure 4.8 where the 255 static DC voltages after the loop is re-locked are used for the predictions flow. The analysis process is based on the methodology of multivariate adaptive regression splines (MARS) [18-20]. The model is first established from given inputs and known outputs. In this work, charge pump current, VCO integral gain, VCO proportional gain, locking time, bandwidth, and phase margin

are to be predicted from the model trained by sensors output DC signatures. A portion of known input matrix is used at the beginning for model learning. Then the remaining parameters will be applied to the model to verify the accuracy. 70 % of the PVT matrixes are provided for the model training. Six sets of integrator static outputs are collected to increase the testing sensitivity from regression models.

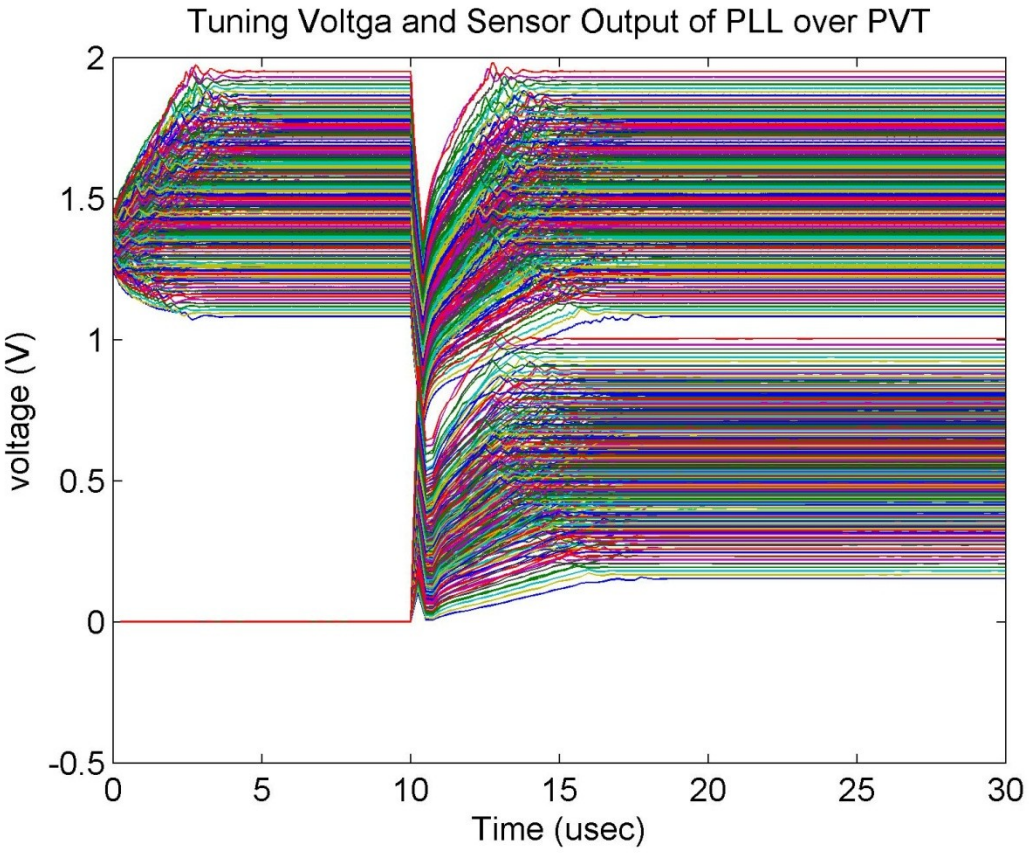


Figure 4.8. The transient waveforms of tuning voltages of VCO in a PLL and integrator output voltages when a reset signal is applied to trigger the detection.

Results of specification prediction are analyzed through MARS algorithm and presented in Figure 4.9 for the six parameters over PVT corners. Projections from the model provide useful information to track these loop dynamic performances. The result for charge pump current achieves the best accuracy. The evaluation of integral, proportional path gain, and locking time provides reasonable precision. Prediction of

bandwidth and phase margin is more diverse than the other analysis but a linear estimation is still demonstrated by the trace.

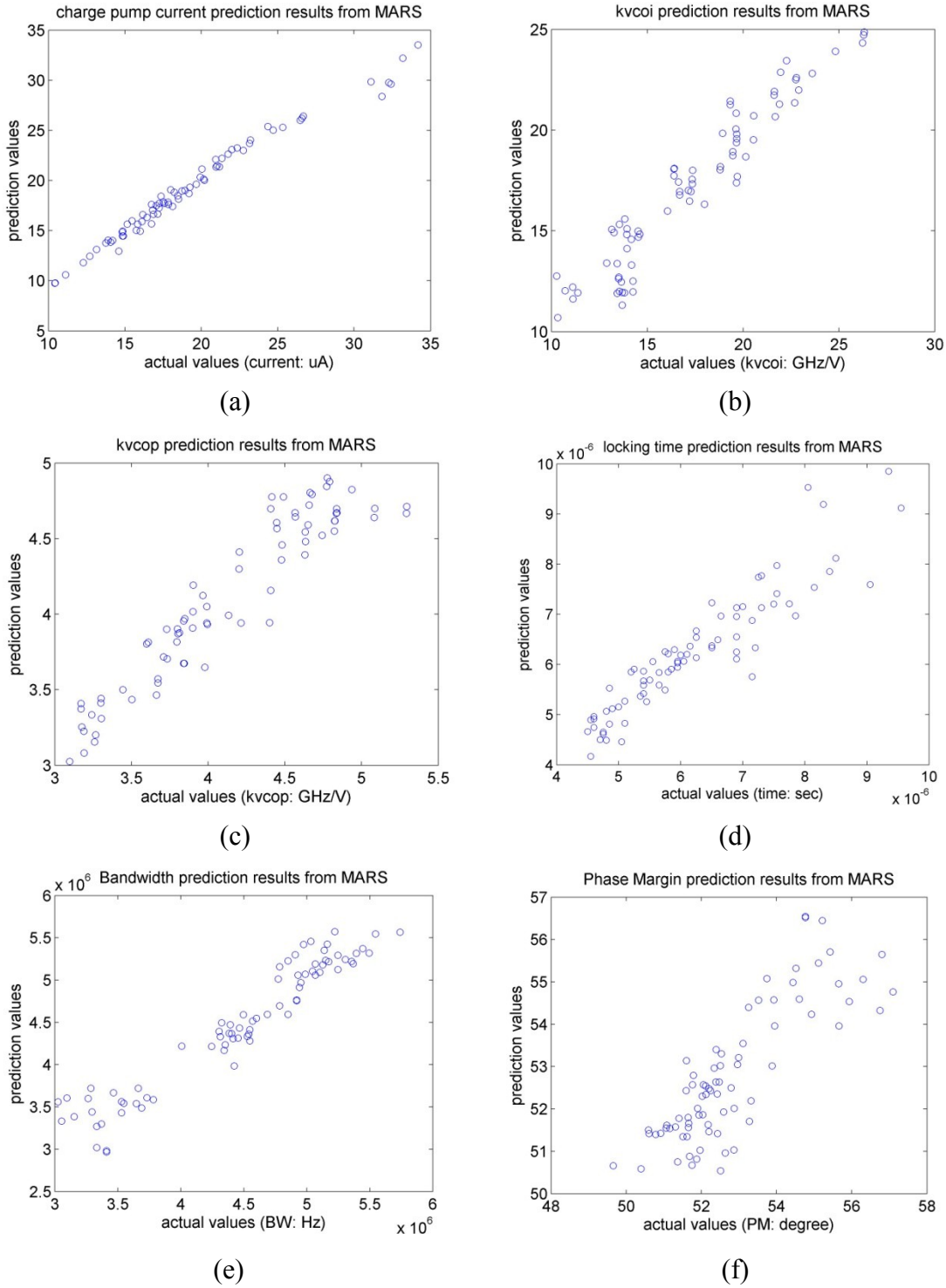
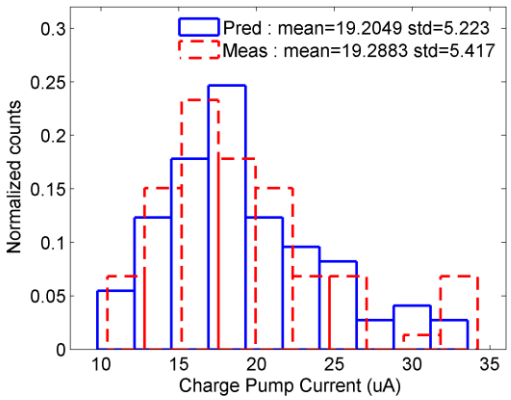
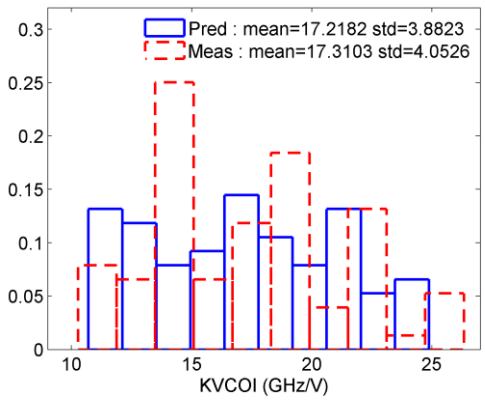


Figure 4.9. Prediction values of six parameters from MARS: (a) charge pump current, (b) VCO integral path gain, (c) VCO proportional gain, (d) locking time, (e) bandwidth, and (f) phase margin. Actual values are acquired from PVT simulations for model training.

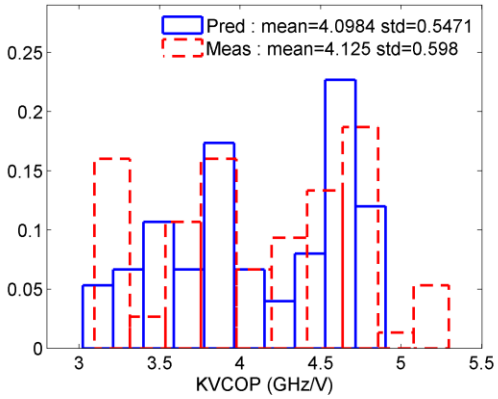
Linear correlation is provided in Figure 4.9 to show the mapping between inputs and outputs while statistic information is capable of summarizing the close distribution from estimated parameters. Further comparison of the predicted values is therefore performed with the statistic number in Figure 4.10 including mean values, standard deviations, and histograms. Statistically the distributions of measured and modeled data are close to the each other.



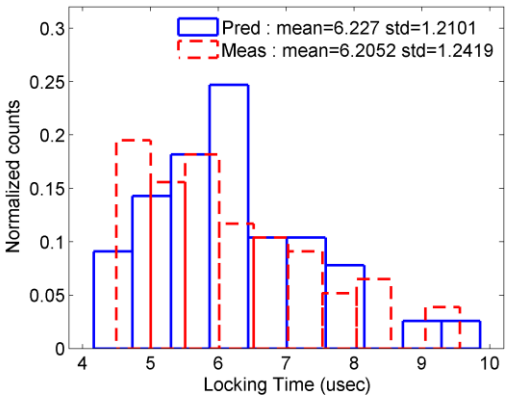
(a)



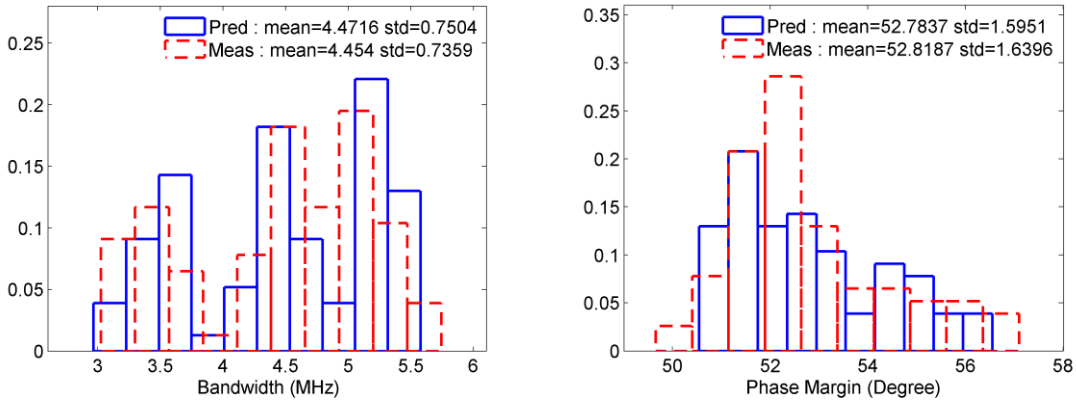
(b)



(c)



(d)



(e) (f)

Figure 4.10. Histogram comparison between prediction and measured values of six parameters from MARS: (a) charge pump current, (b) VCO integral path gain, (c) VCO proportional gain, (d) locking time, (e) bandwidth, and (f) phase margin. Phase Margin. The model provides best estimation and accuracy for charge pump current.

Measurement results of response characterization through the sensor are verified by an integrator attached to a 7GHz PLL evaluation board. The hardware setup is shown in Figure 4.11 where the CUT input reference frequency is modulated by a slow signal to reset the loop locking behavior periodically.

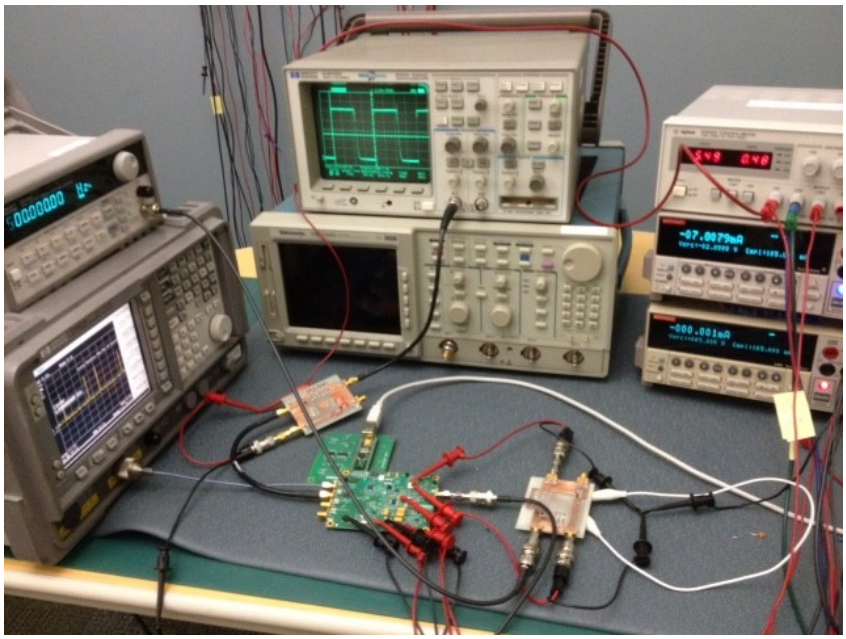
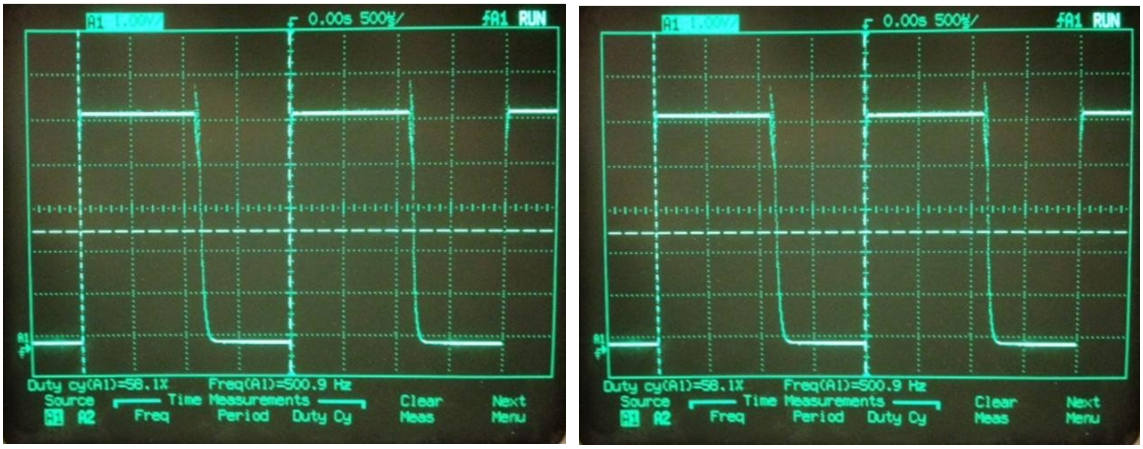


Figure 4.11. The hardware of analog-based sensor test of PLL. A 7GHz PLL is applied for the validation.

The modulation can be monitored on the spectrum as well to validate the CUT is stable given a modulation frequency. The integrator is connected to the control voltage ported from the evaluation board for response extraction.

In this test, the output response is characterized by the integrator with a 500Hz modulation frequency and a programmable charge pump current from 1000 uA to 2500 uA. When a value of charge pump current is programmed and results in different loop bandwidth, it creates various slew rate from the integrator output at the rising edge due to different locking speed. However, at the falling edge of integrator output, the slew rate variation is relatively small since the node is triggered to be strong discharged by the modulation signal. As a result, the duty cycle of integrator output can correlates the input setting of charge pump and the locking speed. Figure 4.12 demonstrates the output duty cycle from different charge pump value.

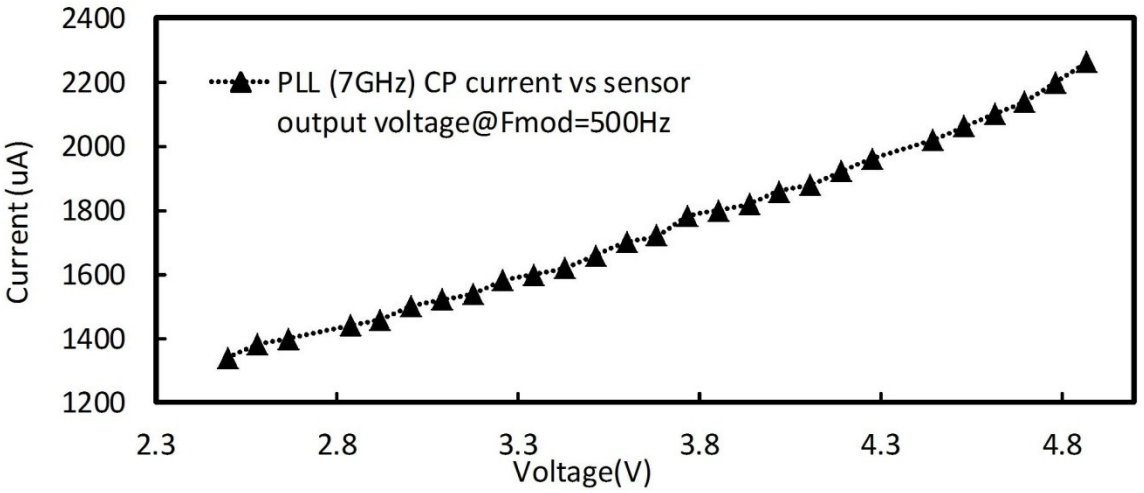


(a) (b)

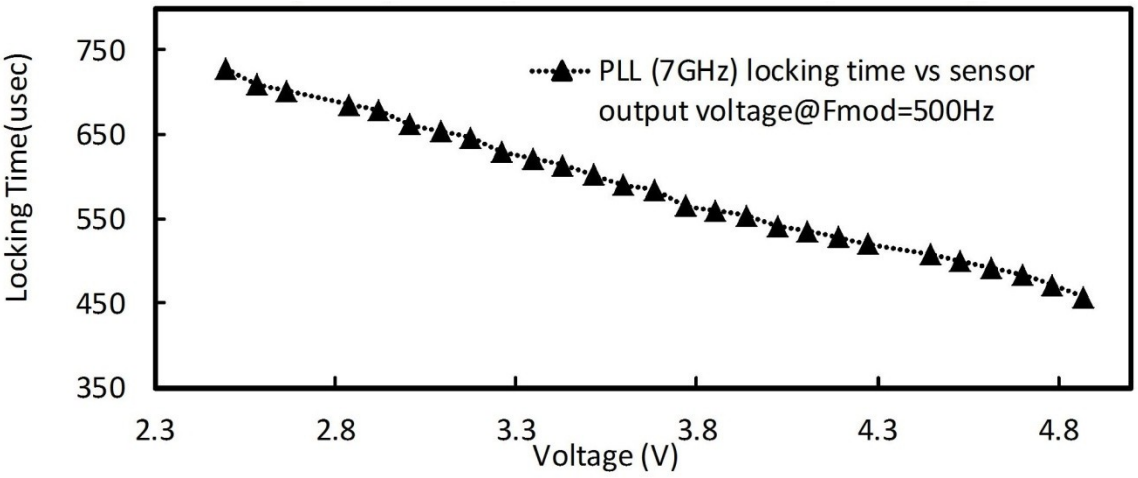
Figure 4.12. The integrator output features different duty cycle from different charge pump current settings of (a) 1960 uA and (b) 2540 uA.

Figure 4.13 are the correlation results of the charge pump current and the locking speed after sweeping the charge pump current. Although the loop bandwidth is unknown

due to the embedded design of the CUT which doesn't allow external access, the locking speed is directly affected by the loop bandwidth and is shown to be correlated in the mapping function closely. The experiment result verifies the analog sensor test methodology for PLL.



(a)



(b)

Figure 4.13. The correlation between the integrator output voltage and (a) the PLL charge pump current (b) the PLL locking speed.

4.3 Analog-based Sensor for Reference Spur

4.3.1 Reference Spur and Static Phase Offset in PLL

The conventional architecture of a PLL with impact from the reference clock is shown in Figure 4-14 which includes a phase frequency detector (PFD), charge pump (CP), voltage-controlled oscillator (VCO), loop filter, and feedback dividers. Reference spurs arise because of the mismatch and nonlinear effect in the periodic signal path from the PFD to the CP. Circuit mismatch existing between the reference and divided feedback path result in charge imbalance. Nonlinear charge sharing and charge injection take place as well in a switch-based current-control circuit like a CP. A finite phase offset occurs in the feedback comparison as a contribution from reference perturbation.

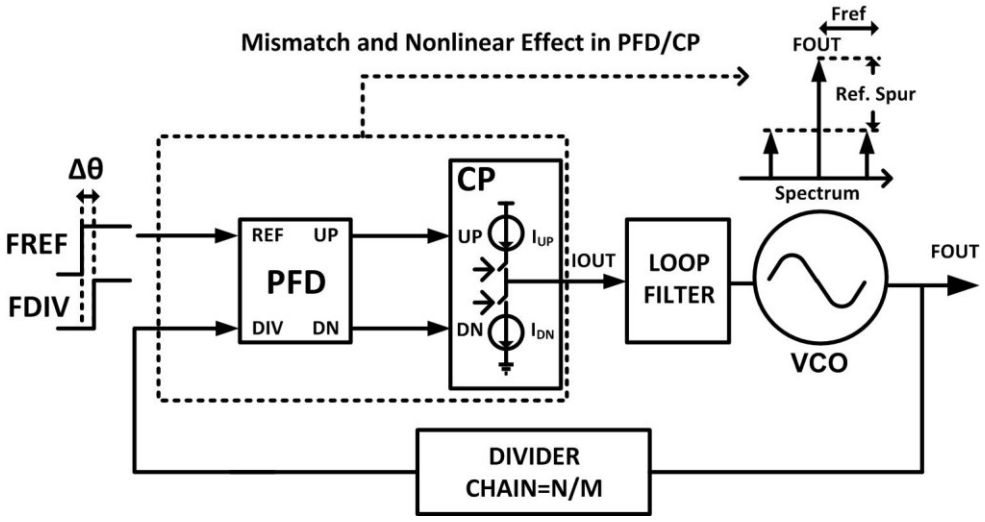


Figure 4.14. The reference spur of conventional PLL concludes the mismatch and nonlinear effect from PFD/CP.

The charge pump PLL in Figure 4-14 also includes a tri-state PFD, ring oscillator, and dividers. Based on (8), the ratio of PLL output spur power P_{spur} due to charge pump current $I(w_{ref})$ relative to output power $P_{carrier}$ can be further expressed as

$$\frac{P_{spur}}{P_{carrier}} = \left(\frac{K_{vco}\left|I(w_{ref})\right|\left|Z(jw_{ref})\right|}{2w_{ref}}\right)^2, \tag{20}$$

where K_{vco} is VCO gain, $I(w_{ref})$ is charge pump current, and $Z(jw_{ref})$ is the loop filter impedance [25]. For a given parameters of PLL, the reference spur degrades when the charge pump current increases based on Equation (20). It is because the ratio of reference frequency to loop bandwidth decreases as a high CP current increases the PLL bandwidth. However, Equation (20) is derived from PLL linear transfer function and doesn't explain mismatch and nonlinear effect. The signature test of reference spur is therefore challenging.

Clearly the periodic events from the charge pump dominate the magnitude of the reference spur as shown in Figure 4.15. When the reference ripples on the control voltage line become large, the reference spur coming from VCO modulation becomes large. A static phase offset (SPO) occurs between PFD UP and DN signal to achieve a charge balance. For a given static voltage at CP output, the net charge is zero and can be analyzed as

$$Charge\ Pump\ Net\ Charge\ Q$$

$$= \int I_{up}dt + \int I_{dn}dt + Q_{up,nonlinear} + Q_{dn,nonlinear}$$

$$= \int I_{up}dt + \int I_{dn}dt + \int I_{up,nonlinear}dt + \int I_{dn,nonlinear}dt$$

$$= \int I_{up,total}dt + \int I_{dn,total}dt = 0\,, given\ a\ static\ CP\ output\ voltage \tag{21}$$

$$\rightarrow \frac{T_{pw,up}}{T_{pw,dn}} = \frac{I_{up,total}}{I_{dn,total}}\,. \tag{22}$$

The reference spur as well as SPO is the total effect contributed from CP current mismatch, layout imbalance, and nonlinear switching effects. As a result the SPO serves

as a target for reference spur detection by carrying important information regarding PLL reference spur performances.

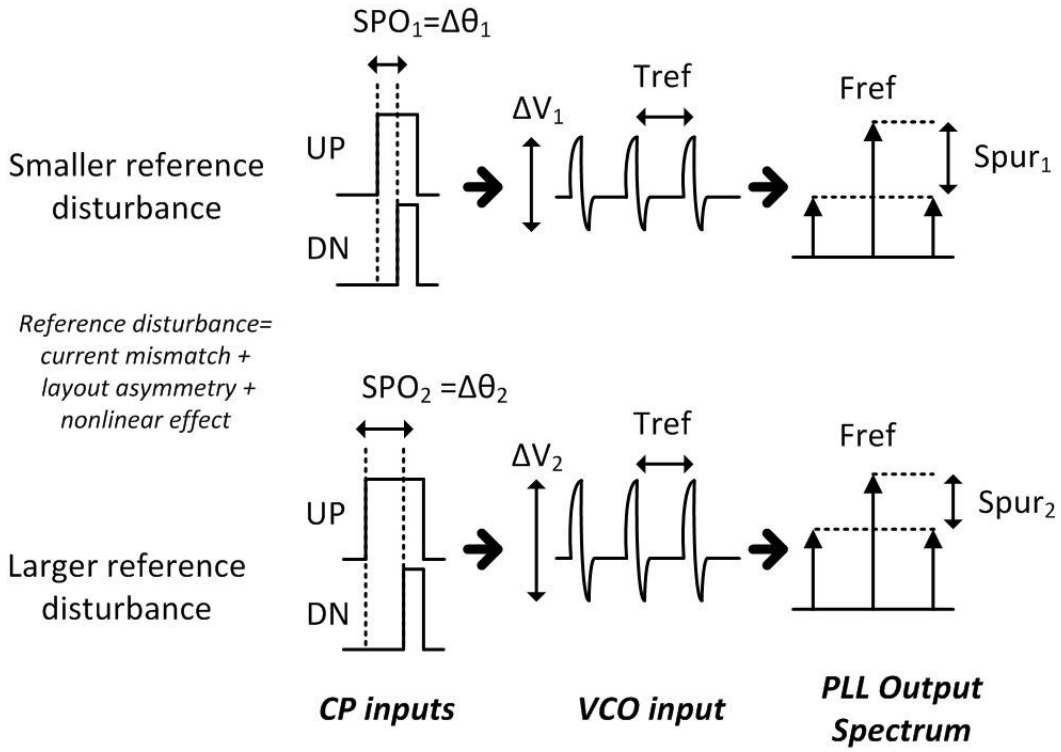


Figure 4.15. The contribution of reference spur comes from current, layout mismatch, and nonlinear effect.

4.3.2 **Sensor Operation and Analysis for SPO Detection**

An integrator is selected as a sensor to accumulate input timing difference for PLL response extraction [49]. The schematic of integrator and the output waveform are shown in Figure 4.16. Since the N-type integrator is ground referenced, it is sensitive to short digital pulses. When the input transistor is active, it operates as a switch to induce current and charge on the output node. In order to shut off the current, an enable transistor is cascoded between the integrator and the rail voltage. The voltage seen at the integrator output due to periodic input pulses can be analyzed by splitting the charge and

discharge activities. When the sensor is activated at PLL steady state, the unit voltage variation Δv_i at the integrator output during the i_{th} reference cycle can be written as

$$\Delta v_i = \frac{\Delta Q_i}{c} = \frac{1}{c} \int \Delta I \cdot dt$$

$$= \frac{1}{c}\left(\int_{t_i}^{t_i+T_{pw}} I_{charge,i} dt - \int_{t_i+T_{pw}}^{t_i+T_{ref}} I_{discharge,i} dt \right)$$

$$= \frac{1}{c} \int_{t_i}^{t_i+T_{pw}} I_{charge,i} dt + V_i e^{-\Delta t / RC}$$

$$= \frac{1}{c} \int_{t_i}^{t_i+T_{pw}} I_{charge,i} dt + V_i e^{-(T_{ref}-T_{pw}) / RC}, \quad (23)$$

where ΔQ_i is the charge accumulated on the capacitor C during the i_{th} reference interval, ΔI which is separated into charge current $I_{charge,i}$ and discharge current $I_{discharge,i}$ is the net current flowing into C, t_i is the starting integration time of the i_{th} reference interval, T_{pw} is the UP/DN pulse width, and T_{ref} is the reference period.

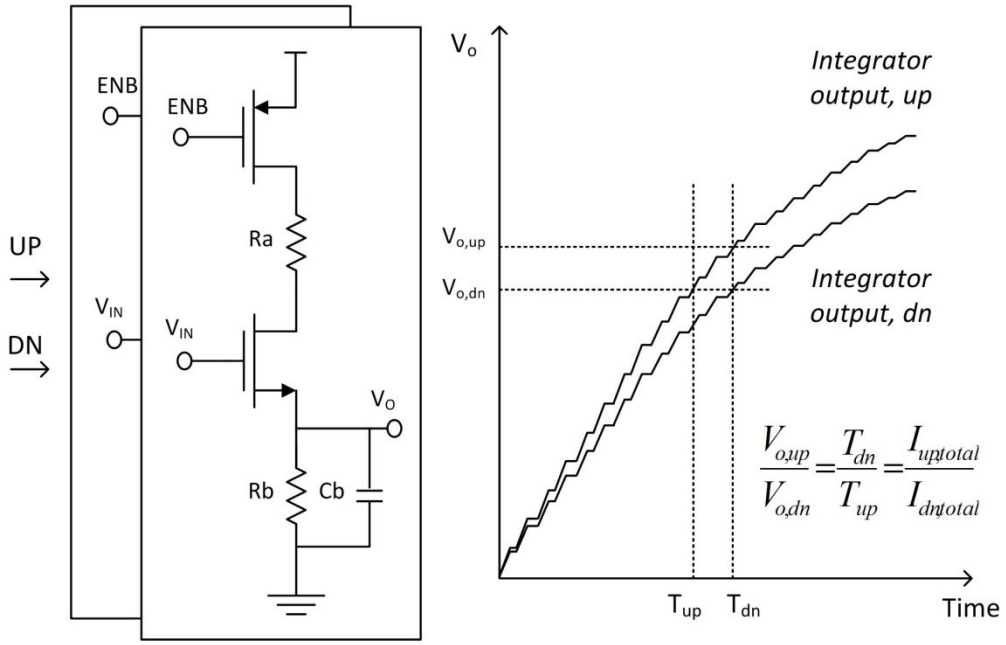


Figure 4.16. The integrator controlled by PFD signals can be used for SPO detection.

T_{pw} is actually the turn-on time which the voltage is accumulated over and T_{ref}-T_{pw} is the turned-off time when the discharge voltage is subtracted from V_i. During turned-off time, it is a simple RC discharge circuit and therefore the integration can be simplified by a transient exponential expression with V_i as the beginning static voltage. Based on Equation (23), the static output voltage $V_{o,static}$ after a long series of reference ripples is expressed as

$$V_{o,static} = \sum_{i=0}^{\infty} \Delta v_i$$

$$= \sum_{i=0}^{\infty} \frac{1}{c} \int_{t_i}^{t_i+T_{pw}} I_{charge,i} dt - \sum_{i=0}^{\infty} V_i e^{-(T_{ref}-T_{pw})/RC}$$

$$= \left(\sum_{i=0}^{\infty} I_{charge,i}\right) \frac{T_{pw}}{c} - \left(\sum_{i=0}^{\infty} V_i\right) e^{-(T_{ref}-T_{pw})/RC}, \qquad (24)$$

where an assumption that the i_{th} charge current $I_{charge,i}$ is constant during the i_{th} period T_{pw} is made for the summation. This charge current is biased through the transistor with a rail input voltage and a slowly changed output voltage at the source terminal. The assumption is made based on the fact the UP/DN pulse is only a small ratio of the reference period. Conventionally the ratio is less than 10% with the pulse width from 1 to 10 nsec. By the time the integrator is activated, the charge current is large because the overdrive voltage is large. Similarly, the succeeding discharge current is small because the output voltage is small. At the beginning phase of integration, the voltage hence ramps fast due to a huge difference between charge and discharge current. On the other hand, a charge balance will be achieved between the on and off interval when a long series of pulses are integrated. At the static stage, the integrated bias current is equal to the released charge. The expression of Equation (24) can be further written as

$$\left(\sum_{i=0}^{\infty} I_{charge,i}\right)\frac{T_{pw}}{c} - \left(\sum_{i=0}^{\infty} V_i\right) e^{-T_{ref}\left(1-T_{pw}/T_{ref}\right)/RC}$$

$$\cong A \cdot T_{pw} + B, \quad \text{as } \mathrm{T_{ref}} \gg \mathrm{T_{pw}} \tag{25}$$

$$I_{charge,i}\frac{T_{pw}}{c} \gg V_i e^{-(T_{ref}-T_{pw})/RC}, \quad \text{as i is small}$$

$$I_{charge,i}\frac{T_{pw}}{c} = V_i e^{-(T_{ref}-T_{pw})/RC}, \quad \text{as i} \to \infty \tag{26}$$

The final integrator output voltage is approximately proportional to the input pulse width according to Equation (24), which can be used for SPO detection in PLL since the pulse width and phase offset remain the same when the loop achieves its steady state. As the waveform shown in Figure 4.16, the output static voltage can be estimated in the rising edge as well. A comparator can be used to determine the timing when a reference voltage is achieved. These detection criteria can be summarized as

$$\frac{T_{pw,up}}{T_{pw,dn}} = \frac{V_{up,static}}{V_{dn,static}}, \tag{27}$$

$$\frac{V_{up,static}}{V_{dn,static}} \approx \frac{V_{o,up}}{V_{o,dn}} \approx \frac{T_{dn@v_{th}}}{T_{up@v_{th}}}, \tag{28}$$

where T_{dn} and T_{up} are the time points when the integrated curves cross a threshold voltage v_{th}. Both the static voltage comparison and the dynamic comparison in Equation (27) and (28) are used for SPO detection and are introduced in the following sections.

For loop parameters, the integrator senses the response as well since the pulse width carries the information regarding PLL dynamic behavior. The output voltage also serves as a signature extraction for locking time, charge pump current, loop bandwidth, and phase margin.

4.3.3 **BIST for SPO Estimation**

Since the static phase offset is proportional to the integrator output voltage, the integrator in Figure 4-16 serves as the fundamental element for SPO estimation. A BIST architecture in Figure 4-17 is proposed to extract the time-to-voltage information via the help of comparator and clock counter [49]. Both are simple circuits and feature low overhead in area and power. The operation and verification results are presented in the following discussions.

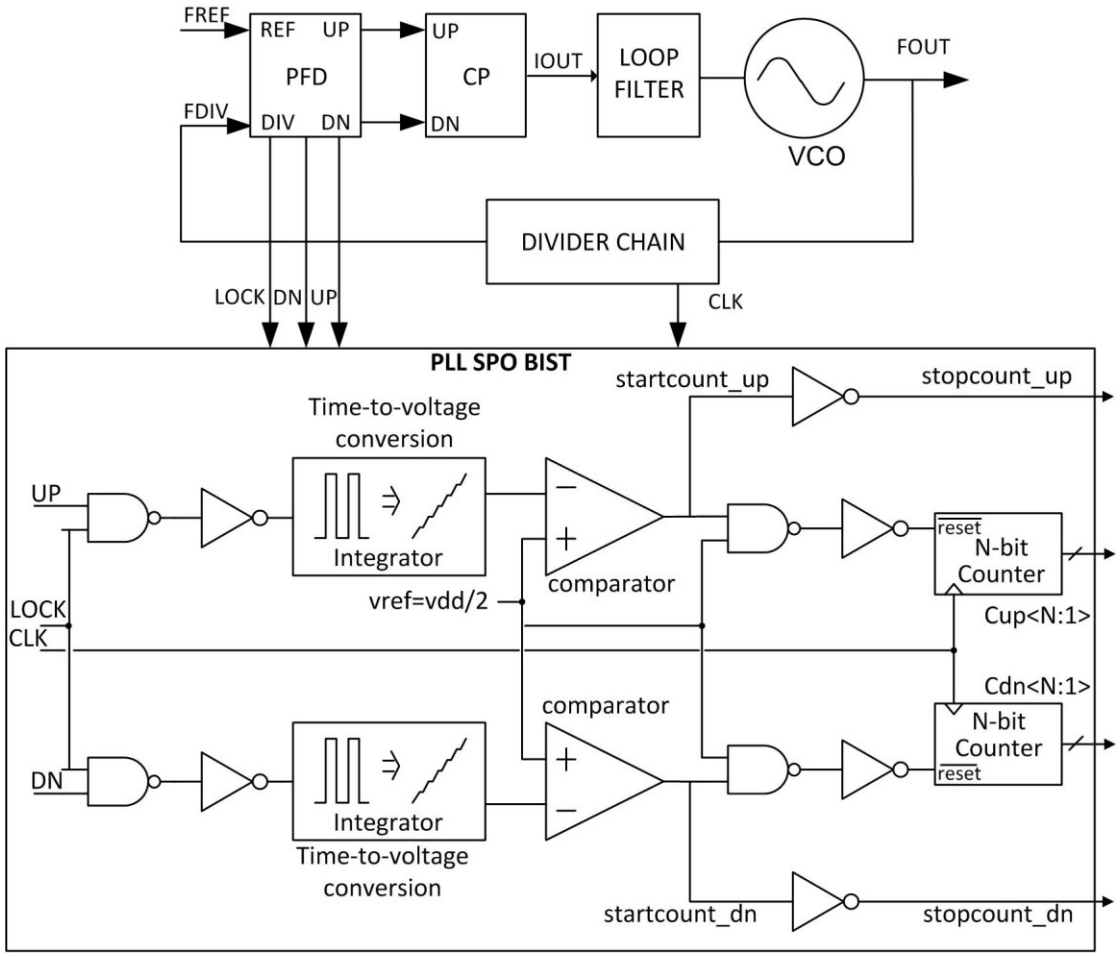


Figure 4.17. BIST including integrators, comparators, and clock counters for SPO estimation features only digital connection with the PLL.

4.3.3.1 BIST Architecture

The BIST interface with PLL makes RTL-based implementation possible via including only digital signals, namely UP, DOWN, LOCK, and CLK. These digital signals can be distributed securely in SoC without affecting analog performances. This self-test circuit starts operation only when the PLL is steady, which is monitored by the LOCK signal from PFD. The clock counter is turned on when the LOCK signal goes high. A reference voltage is selected as a threshold for comparison between the two integrated curves. As long as the outputs cross the threshold value, the following counter is triggered to stop the counting. The architecture takes advantage of the comparators to obtain the information of switching time. CLK is a know frequency source from clock division in the PLL feedback divider chain after the loop is locked. For a high resolution, a fast clock from PLL is required. However, a trade-off exists between the clock speed and the counter operation limit.

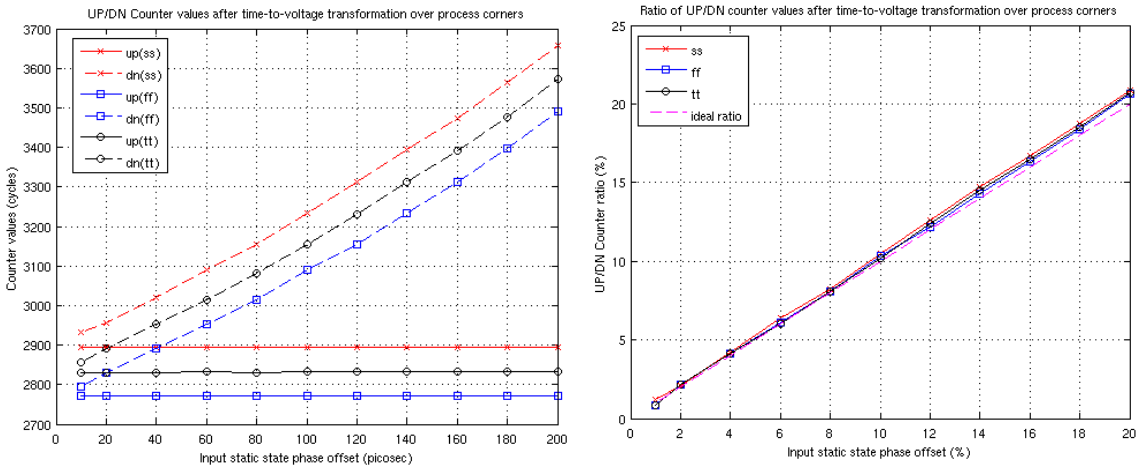
Based on (28), Figure 4-17 compares the transition edges of integration curves instead of static values because the output has a higher conversion gain during transition and a higher sensitivity for response extraction. Once the output is settled, the difference between the TWO path is less detectible. For a comparator, it is preferred for mid-range operation due to its dynamic range constrain as well. This system achieves a small power overhead since the comparator and digital logic both are able to be disabled after comparison.

4.3.3.2 Test Cases and Simulation Results

The BIST is implemented in CMOS 45nm process to test its performances over process corners. UP and DN pulses are created with a range of static phase offset as input

stimulus at a period of 50MHz. The SPO ranges from 1% to 20% of a 1nsec pulse width. A self-biased five-transistor PMOS amplifier is used as the comparator. Two 12-bit clock counters are used. The reference voltage of the comparator comes from a diode-connected voltage divider sourced by the supply voltage. The current consumption of comparator is less than 10uA. Figure 4-18(a) is the simulation result showing linear correlation between UP and DN counter output values and the input static phase offset over SS, TT, and FF. In this test bench the SPO occurs in the DN pulse. The flat and solid curves present the UP counter output with a fixed pulse width. However, the mismatch may happen at the UP pulse in reality and swap the result.

Figure 4-18(b) shows the correlation between counter outputs and the SPO ratio by calculating the output offset ratio. The SPO ratio is clearly tracked by the counter output offset ratio across different process corners.



(a) (b)

Figure 4.18. BIST output results: (a) UP and DN counter output values over SS, FF, and TT corners. (b) Division of the counter values provides linear tracking with the SPO.

This section proposes a BIST for SPO estimation by comparing the transient integration curves. A close correlation of BIST results is shown for the SPO. The total

current overhead is less than 200uA. Two capacitors of 100pF are required at the two integrator outputs for an adequate time constant. Further development applying the integrator is done for PLL reference spur estimation in the next section.

4.3.4 **Testing Methodology for Reference Spur**

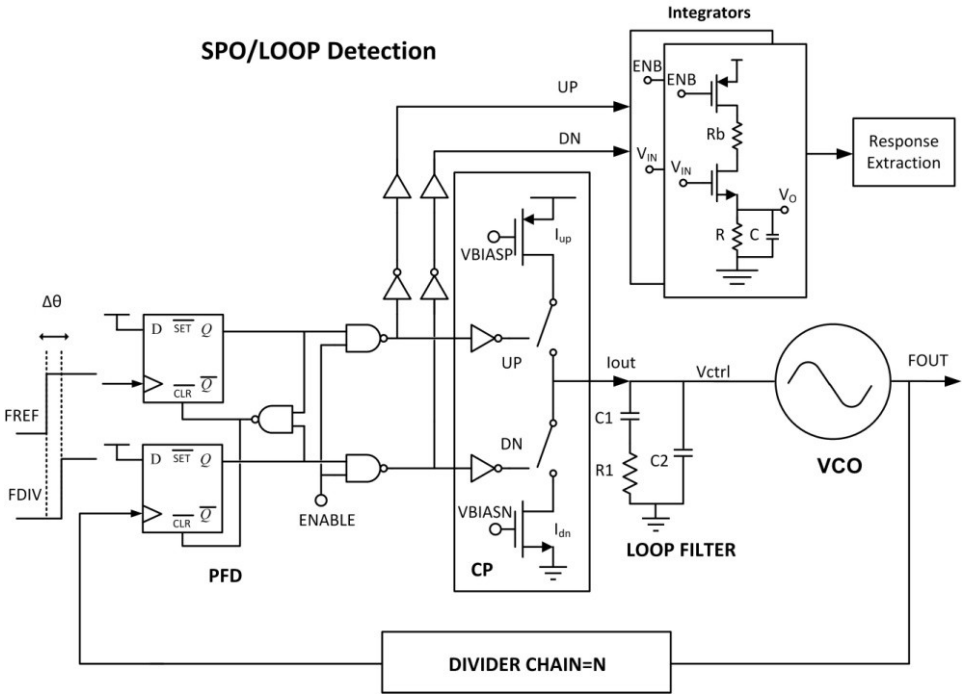
The integrator is used as the same sensor for both reference spur and loop parameters estimation. However, the testing architectures for the two specifications are slightly different. While the reference spur is measured at the static state when the loop is locked, the loop parameters including locking time, charge pump current, bandwidth, and phase margin describe the feedback loop in a dynamic manner. For reference spur the loop response is captured at steady state. For loop behavior, the response can be captured either at steady or transient state. These cases and testing methodologies are discussed in this section.

Figure 4.19(a) shows the PLL architecture applying the integrators for reference spur and SPO estimation. The effect of reference ripples is extracted for estimation after the loop is stable. Instead of comparing the integrator transient output, the output DC values are directly used for SPO and reference spur evaluation. The architecture is simple and doesn't require additional circuits for response extraction. In production test, the output DC values can be easily sampled by ATE with a lock signal as a trigger.

A hardware design of PLL in Figure 4.19(a) is implemented in PCB with a tunable charge pump as well. By varying the UP and DN current respectively, not only the charge pump current but also the current ratio is tunable so that the resulting SPO and reference spur are changed. The integrator therefore senses different response for evaluation. In a previous work [50], the correlation between reference spur and SPO via

trimming the charge pump current ratio has been verified across different chips and is shown in Figure 4.19(b).

(a)



(b)

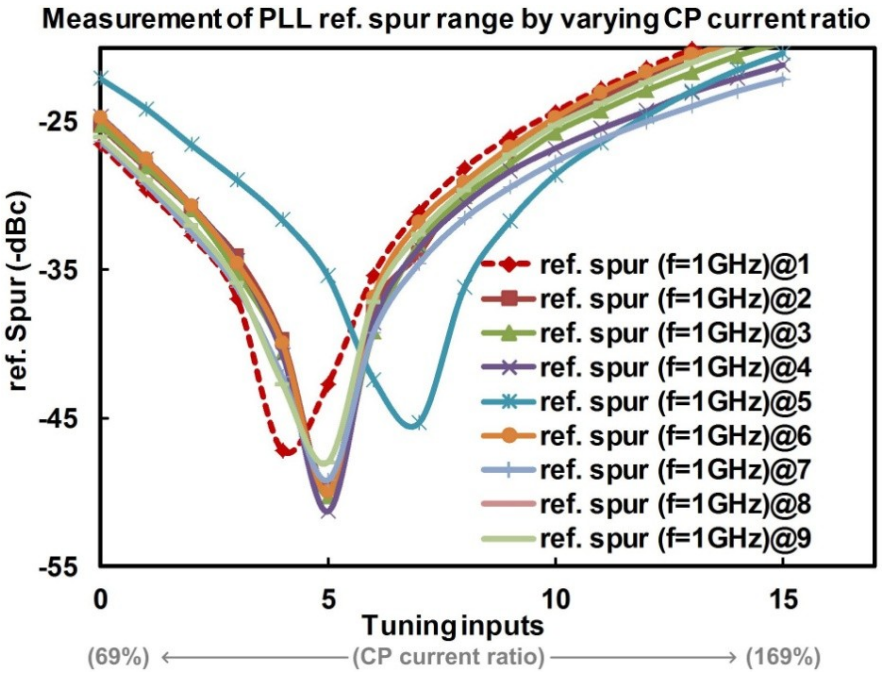
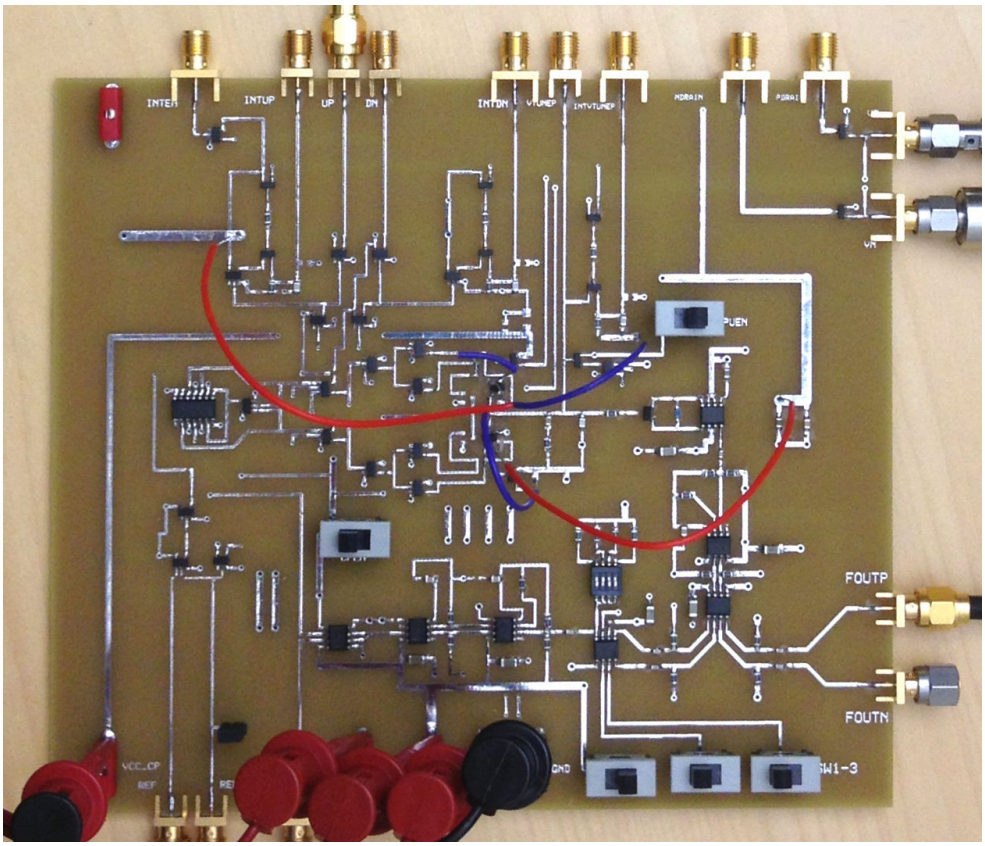


Figure 4.19. (a)BIST including integrators, comparators, and clock counters for SPO estimation features digital connection with the PLL and static detection. (b) The feasibility of varying reference spur by changing the CP ratio is shown.

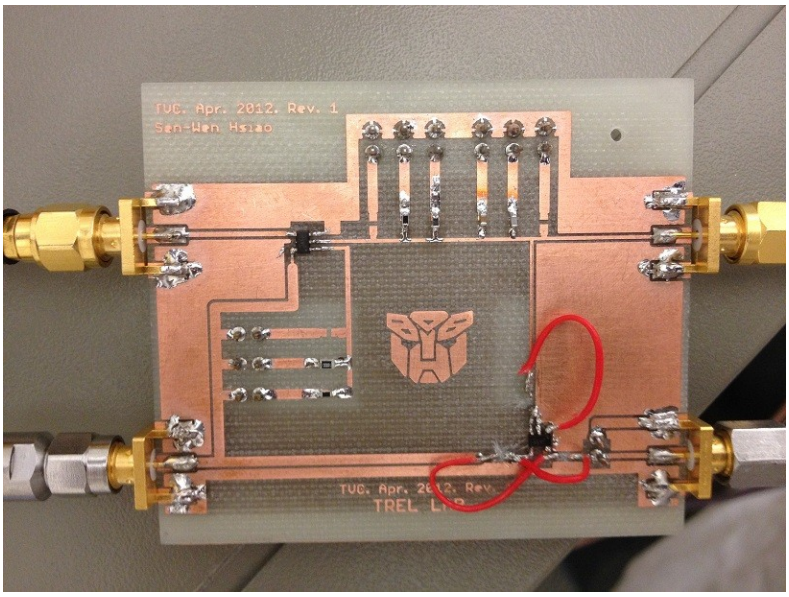
In the figure, the CP ratio (calculated by UP divided by DN current) is changed from 69% to 169% with the best performance of reference spur appeared at the middle between the two extreme biased current ratios.

4.3.5 **Experiments**

The PCB of PLL and integrators are shown in Figure 4.20. At the steady state, the reference spur can be adjusted by CP current ratio, namely VBIASN and VBIASP of this design in Figure 4.19(a). The test flow is described as follows: First, the CP ratio is varied both increasingly and decreasing based on the optimal setting of CP current. One of the bias voltages is used to achieve the purpose. Second, the SPO and reference spur are observed as the output specifications. Finally, the integrator output DC voltages are recorded for response evaluation.



(a)



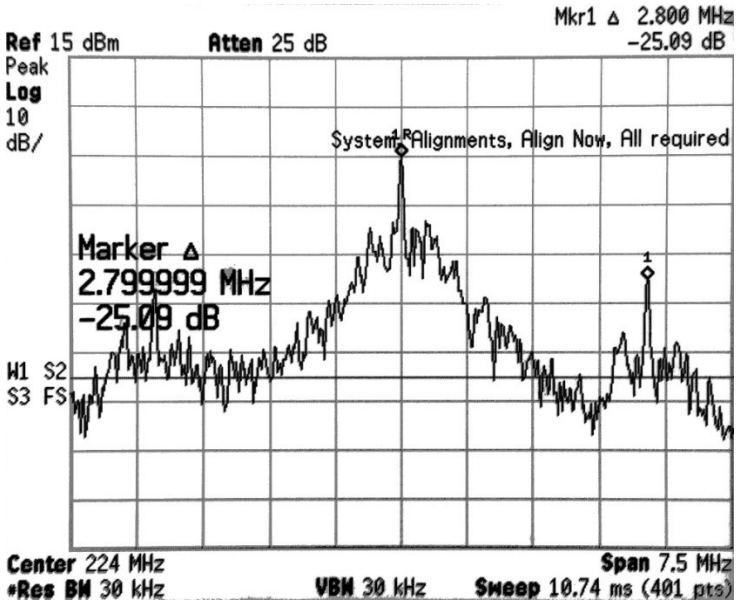
(b)

Figure 4.20. The PCB of (a) PLL with tunable CP and (b) Integrator are shown for reference spur, SPO, and loop detection.

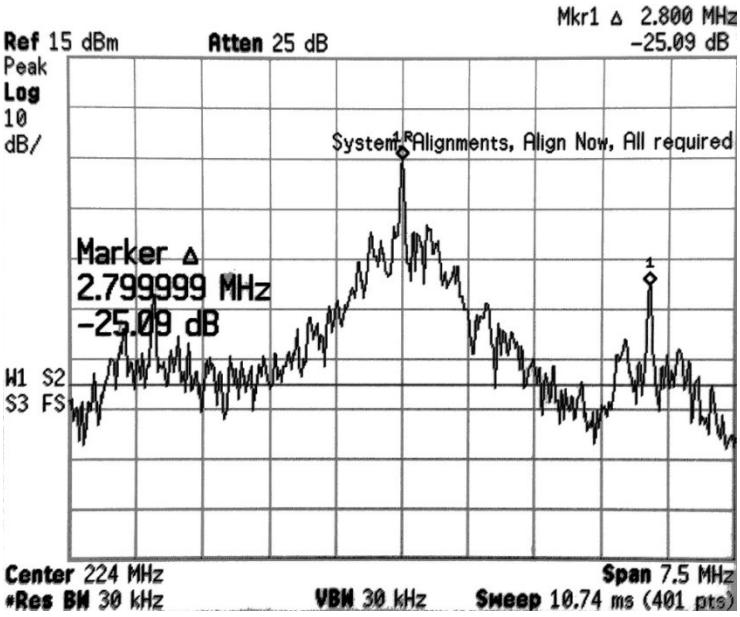
Figure 4.21 shows the optimal and extreme case of reference spur on the spectrum when sweeping the CP ratio. The PLL is locked at 224MHz with a 2.8MHz reference clock. When the reference tone becomes serious, the corresponding static phase offset increases toward extreme directions as well. The waveforms of optimal-matched and two unmatched SPO are demonstrated in Figure 4.22. The performance of reference spur is centered at the case with a matched SPO and degraded toward one and the other direction.

The integrator is attached to the PLL UP/DN signal for output DC value observation on the oscilloscope when changing the CP current ratio. The offset between UP and DN path is tuned from the largest lagging phase to the largest leading phase by varying one of the bias voltages. As a result, the difference between two integrator outputs tracks the SPO variation since there is only one pulse edge and thus one integrator output moved at a time. Figure 4.23 shows the correlation among reference

spur, SPO, and integrator outputs difference under different reference frequencies. It should be noted the PLL has a better reference spur performance when the reference frequency and thus the loop bandwidth is higher.

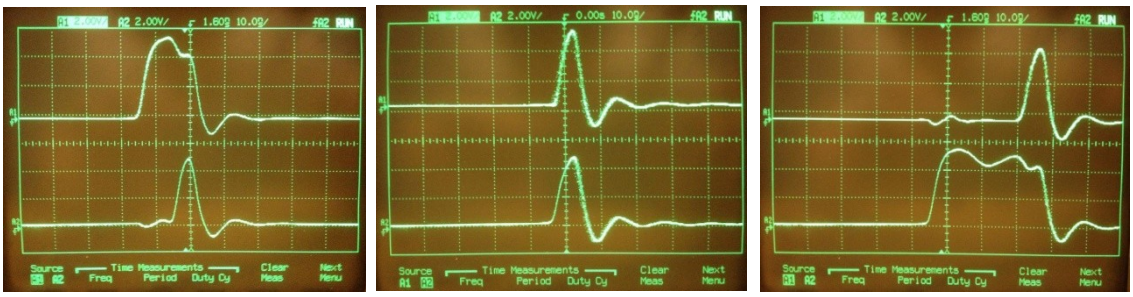


(a)



(b)

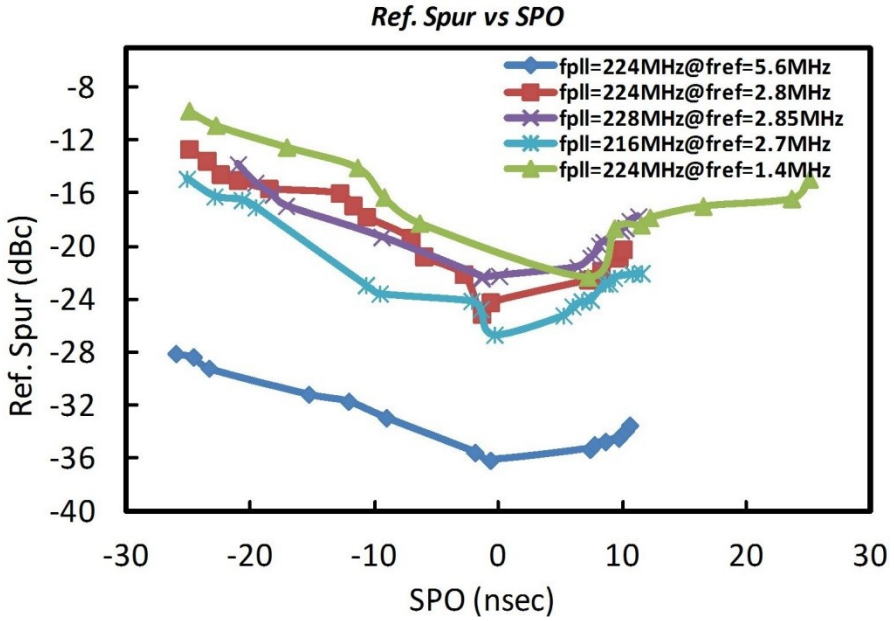
Figure 4.21. The reference spur after adjusting the CP current ratio is shown. (a) The result with optimal SPO. (b) The result with worst SPO.



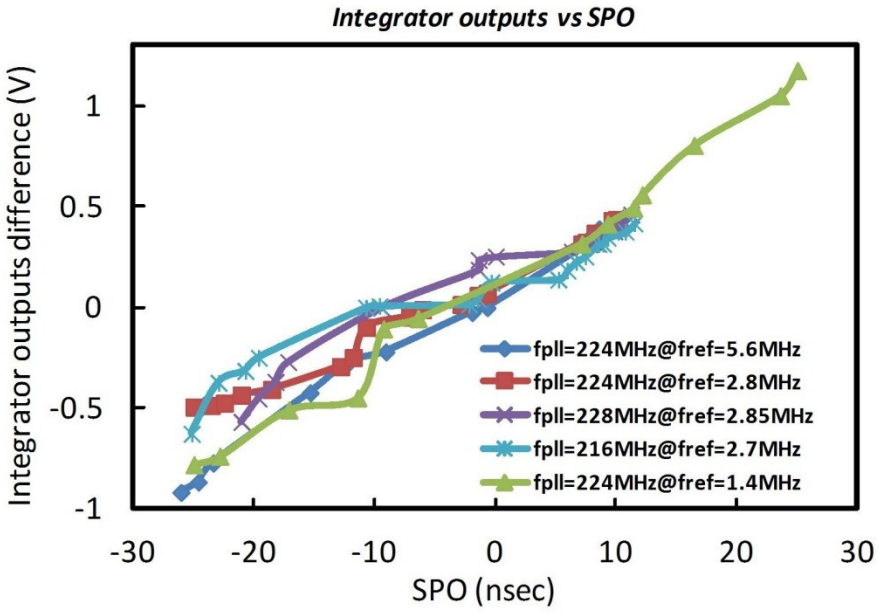
(a) (b) (c)

Figure 4.22. The waveforms of UP (top) and DN (bottom) pulses are shown with different cases: (a) UP pulse is leading DN pulse, (b) UP and DN pulses are approximately matched, and (c) UP pulse is lagging DN pulse.

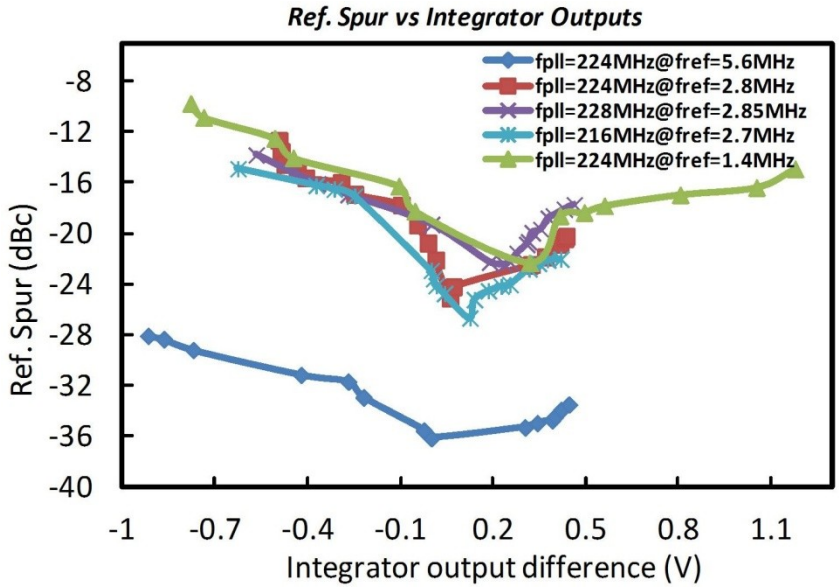
The plots in Figure 4.23(a) and Figure 4.19(b) share similar distribution of reference spur because an optimal value exists between two worst current ratio. The purpose of the sensor testing is to detect the reference spur by integrator outputs. Figure 4.23(b) shows integrator outputs difference mapping the SPO response linearly. Consequently, a correlation between reference spur and integrator outputs difference is obtained in Figure 4.23(c) similarly as Figure 4.23(a) and validates the integrator-based testing.



(a)



(b)



(c)

Figure 4.23. The measured results of reference spur, SPO, and integrator outputs under different PLL inputs are shown: (a) the reference spur are varied versus SPO variation; (b) the integrator outputs difference is tracked linearly by the SPO; (c) the mapping between reference spur and integrator output difference can be obtained.

Performance-wise, the PCB PLL suffers nonlinear effect from the discrete components. Charge sharing and charge injection of switches are serious due to the huge

loading capacitance from the components. The charge pump current is not controlled well, either. However, the test function is still verified by the integrator for PLL reference spur and loop parameters. Such nonlinear impact can be mitigated when an on-chip solution is utilized.

4.4 Summary

This chapter presents an analog-based integrator as a sensor for PLL loop parameters and reference spur testing. The principle of integrator is introduced and further analyzed for the effect of static phase offset in PLL. For the sensor testing, different CUT architectures are introduced with the sensor attached to the PLL. While the SPO response is extracted from the PFD outputs for reference spur evaluation in a steady state, the loop response is evaluated either from the UP/DN signal and PLL control voltage.

For loop parameters testing, the sensor can be used in response extraction for supervised learning methodology. A complete PVT corners are applied in simulations with close correlation for the parameters prediction.

For reference spur testing, a BIST architecture featuring digital interface is proposed for SPO estimation with simulation verification. In addition, a PCB design including a PLL and integrator is proposed.

Hardware measurement results including the PLL and integrator are both provided for validation. The PLL reference spur and loop parameters are correlated linearly by the integrator output, which consequently provides useful information in production test and serves as a fundamental circuit for BIST and calibration design.

CHAPTER 5: CALIBRATION CIRCUITS FOR REFERENCE SPUR

5.1 PLL with Built-in Circuits for Reference Spur Calibration

The proposed charge pump PLL with calibration circuits is shown in Figure 5.1 including a tri-state PFD, ring oscillator, and dividers. The PLL output reference spur power due to charge pump current is described by (19) which implies an appropriate control of the charge pump current and current ratio can adjust the reference spur.

The current ratio R of the charge pump and spur performance of the PLL can be selected by N-bit inputs while the static phase offset detector indicates if the phase between the charging and discharging path is leading or lagging. The off-chip calibration will simply select the optimum point by sweeping all the inputs and verifying the results from the detector.

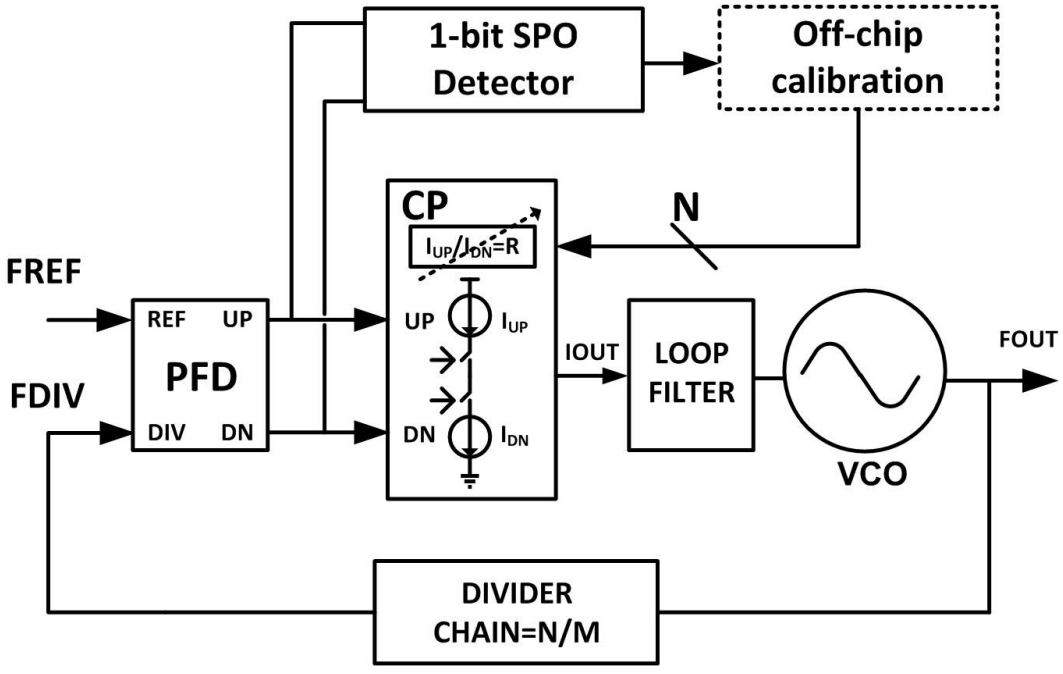


Figure 5.1. Proposed PLL with calibration circuits for reference spur suppression.

Reference spur is a combined result with contributions from mismatch and nonlinear effects of the PFD/CP. The programming of charge pump current can also be viewed as a concluded effect to identify the relationship between the contribution and output spur.

5.2 Detection and Correction Circuits

5.2.1 SPO Detection

Figure 5.2 is the schematic of the SPO detector, which includes a D flip-flop with compensated clock-to-Q delay. A D flip-flop is triggered by a clock edge to sample the incoming signal. In this case, the circuit can differentiate the phase offset between the charge and discharge signals given the time difference is recognizable. There may still be delay mismatch existing for the D flip-flop, but the resolution would be enough if the PLL is operated with finite phase offset and the charge pump has an adjustable step. In conventional PLLs, a phase offset larger than 20 psec is enough for detection.

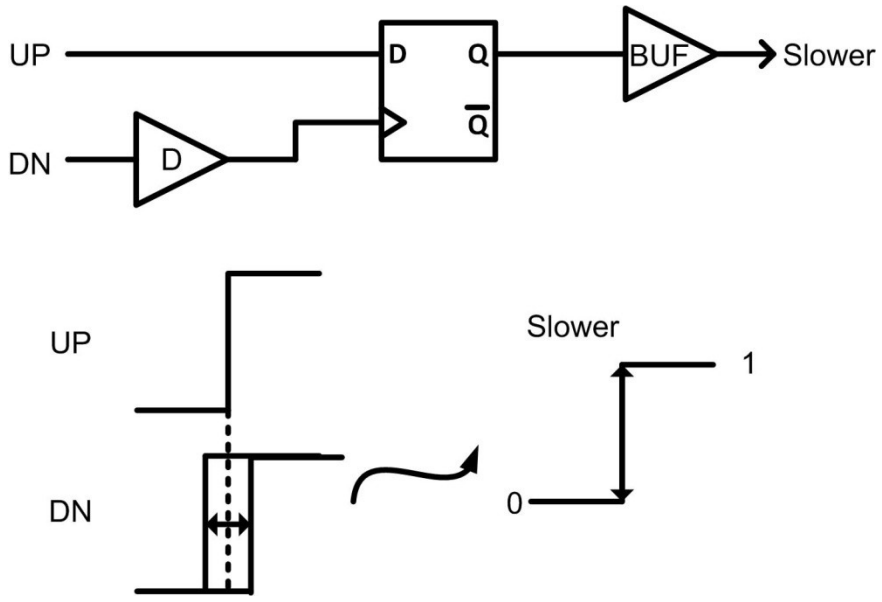


Figure 5.2. The D flip-flop serves as a phase offset detector. When the incoming signal has a reasonable range of time difference, it has the ability to identify the offset logically.

5.2.2 **Charge Pump Trimming**

The charge pump circuit is shown in Figure 5.3. In order to trim the current ratio, the discharge path is designed with current programmability. The cascoded current source of discharge signal is arranged as multiple unit devices MN3<M:1> and controlled by digital logic. To save on headroom of the switch devices, MNen2<M:1> are sized with small voltage drops beneath the current source. The number of elements mirrored is selected by the enable bus selects while the output path is operated with fixed biased devices and dummy switches. If an M-element output trimming element N and n are given, the maximum and minimum discharge current can be expressed as

$$I_{dn,min} = I_{up} \cdot \frac{M}{M+N}, \tag{28}$$

and the ratio of discharge current to charge current can be calculated as

$$\frac{I_{up}}{I_{dn}} = 1 + \Delta\frac{I_{up}}{I_{dn}},$$

$$\Delta\frac{I_{up}}{I_{dn}} = -\frac{n}{M} \sim +\frac{N}{M}. \tag{29}$$

With an appropriate design, the ratio covers a range to match the variation in fabrication. An additional delta-sigma modulation (DSM) is provided for a finer resolution on the trimming current.

The control of charge pump is equivalent to modulating the bias voltage of the current source. The devices are designed to operate in the saturation region under both the maximum and minimum bias condition so that current mirror remains valid. In this design, M equals 16, N equals 11, and n equals 4.

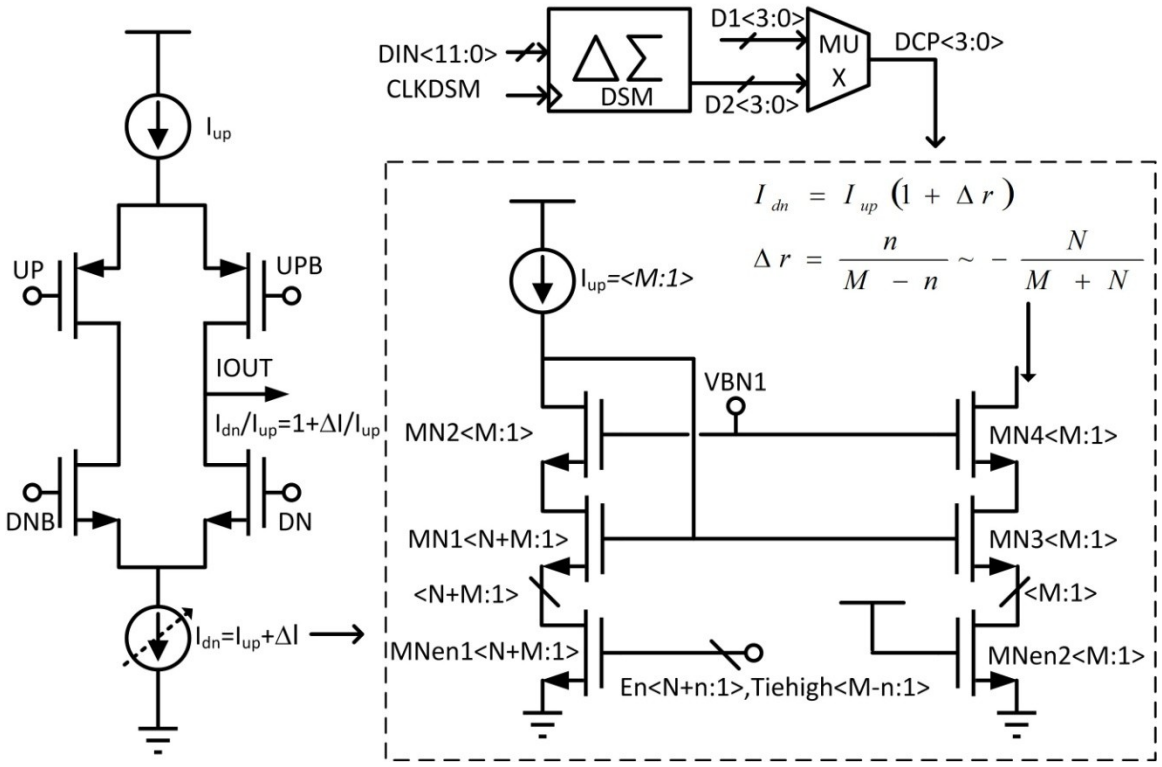


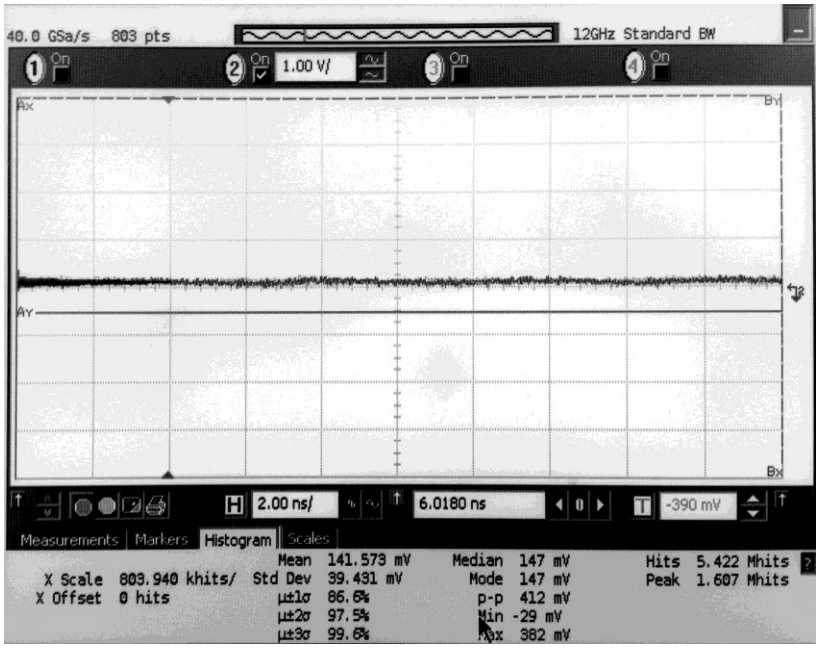
Figure 5.3. PLL charge pump with an adjustable ratio of charge (UP) to discharge current (DN). Delta-sigma modulator provides a higher resolution than direct trimming.

5.3 Experiments

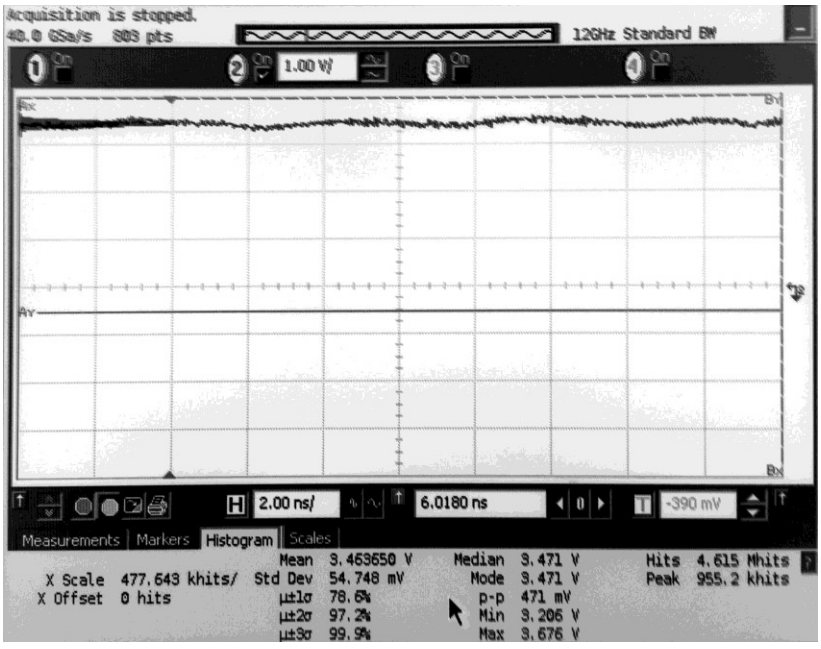
5.3.1 Measurements of Calibration Circuits

The SPO detector provides one-bit resolution. A four-bit word is used to control the 16 steps of the charge pump. The measurement starts from sweeping the charge pump control word and observing the detector output values. In the PLL, the digital output starts from continuing 0 and ends in 1, while the discharge current varies from large to small values. As the current matching gradually changes, the reference spur is also adjusted. An optimum value of reference spur exists in the setting. The purpose of the measurement is to find the last 0 and the first 1 logically at the output of the detector. These outputs are monitored on the oscilloscope as shown in Figure 5.4. The digital oscilloscope is used to determine the last 0 and the first 1 versus calibration setting. An

on-chip state machine can be implemented with this verification. However there wasn't enough time and we wanted insight into this behavior.



(a)



(b)

Figure 5.4. The transient waveforms of static phase offset detector output in a PLL with (a) the last zero and (b) the first one on the oscilloscope.

The default current setting of the charge pump is designed for optimal performance within its adjustable range. In measurement, the default CP value matches the last 0 of the detector output and the optimal value matches the first 1 of the output practically.

Reference spur is monitored on the spectrum analyzer as the charge pump settings were varied. As the current ratio is gradually changed from the one extreme value to the other, the magnitude of the reference spur of the PLL will approach the optimal number and then be degraded again. The reference spur corresponding to the default charge pump and optimized setting is shown in Figure 5.5 for 1GHz and 500MHz outputs, respectively. At 1 GHz, the reference spur is -40.6 dBc before trimming the CP ratio and becomes -53.46 dBc afterwards. At 500 MHz, the reference spur is -29.25 dBc before optimization and then is improved to -52.24 dBc. Improvements of 12.86 dB and 22.99 dB are obtained for different frequency synthesis. Figure 5.6 demonstrates the effect of reference spur on noise with the RMS jitter integrated from the phase noise profile after optimization. The RMS jitter is 9.97 psec and 8.49 psec before and after the trimming is applied for 1 GHz PLL output. The integrated period is from 10 kHz to 10 MHz. For 500MHz, the RMS jitter is 25.09 psec and 18.5 psec, respectively.

The results from sweeping the settings show that the reference spur can be trimmed by finding the first 1 from the output of the detector. The best performance of reference spur occurs at the time when the discharge path has slightly less current than the charge current. This performance matches the design of the PLL. When the PLL synthesizes a low frequency, the CP is biased at a small current and the tuning voltage is locked at a low voltage. While low current makes the circuit matching worse, low voltage

makes the charge injection of discharge path from the switching signals worse than the charge path. Compared with a high frequency loop, the situation is more obvious and can be verified in Figure 5.5.

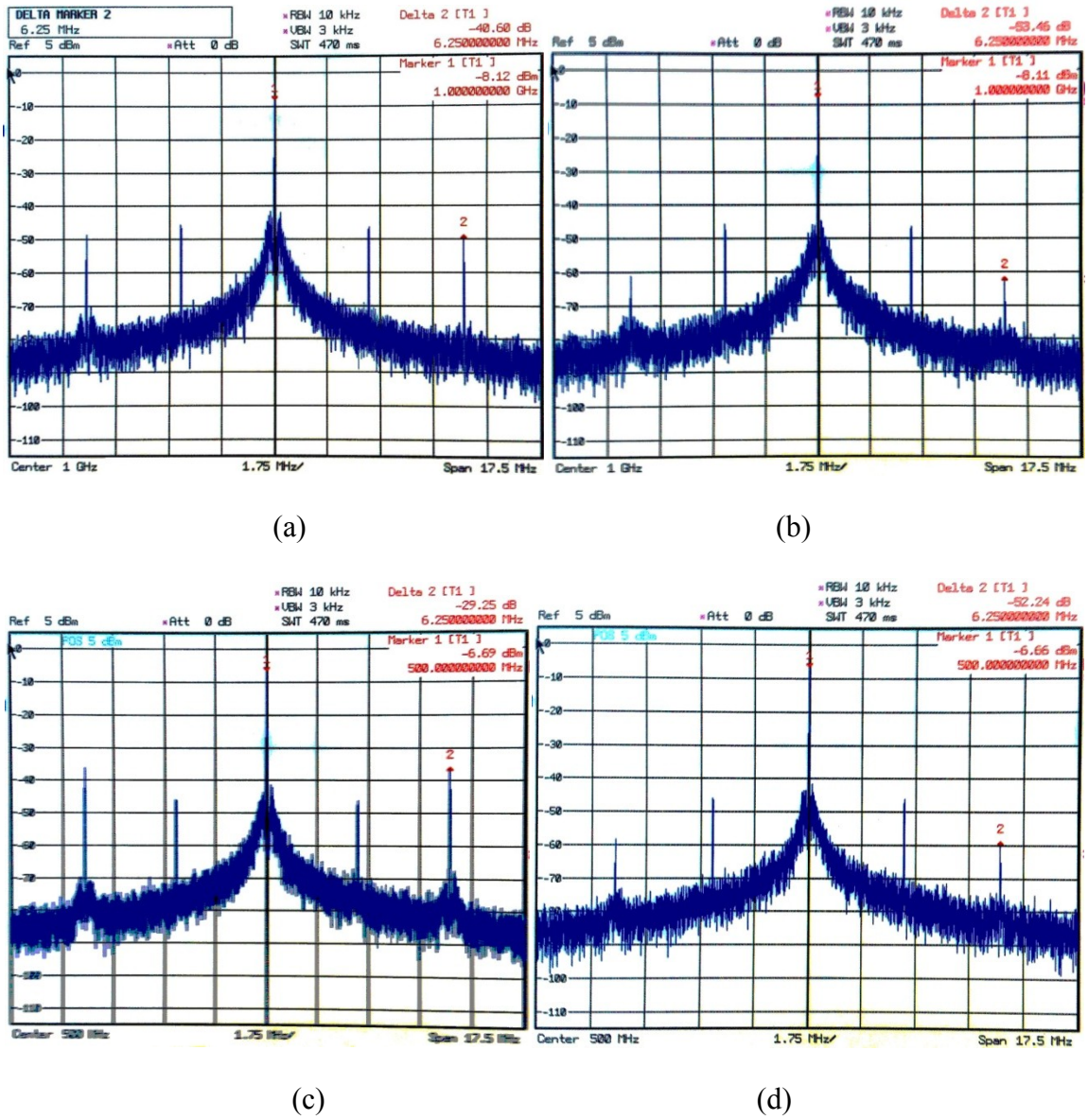


Figure 5.5. The reference spur is improved on the spectrum for output frequency of 1 GHz and 500 MHz. (a) 1GHz PLL output without CP optimization. (b) 1GHz PLL output with CP optimization. (c) 500MHz PLL output without CP optimization. (d) 500MHz PLL output with CP optimization.

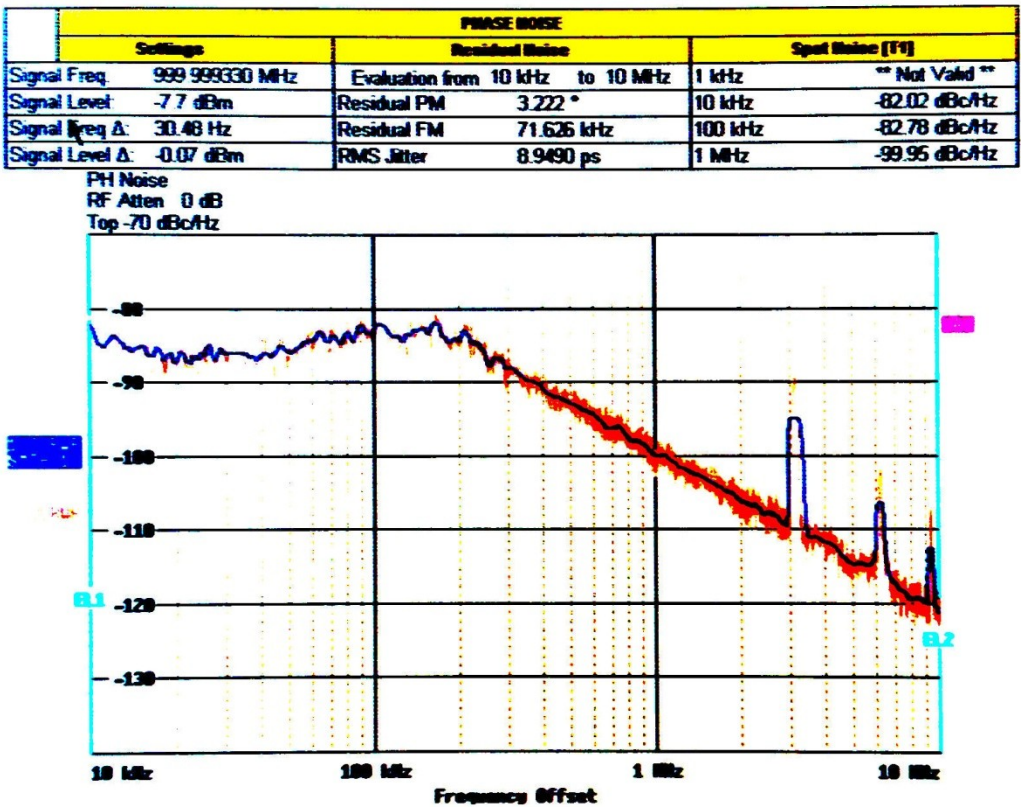


Figure 5.6. Integrated RMS jitter of 1GHz PLL output after CP optimization from 10 KHz to 10 MHz.

The PLL features both fractional and integer synthesis. In fractional mode, the fractional ratio of output frequency is controlled by a 24-bit word with microdegree resolution [51]. In this paper, the reference frequency is 6.25MHz for synthesizing 1GHz and 500MHz outputs in integer mode. Figure 5.5 and Figure 5.6 have a spur at half of the reference frequency which is generated in the IO circuit for additional test purposes and did not originate from the PLL. The improvement is focused on the correct reference frequency tone.

5.3.2 **Calibration Results of PLL**

The PLL outputs a clock with current ratio adjustment in the CP. The tunable range of reference spur performance is shown in Figure 5.7. Different synthesized

frequencies are measured to validate the circuit technique. The result from DSM is shown with a fine resolution as well. A minimum range of 15dB is available from 400 MHz to 1 GHz. In an application to test the tolerance of long-term jitter or reference spur on an adjacent channel, this circuit can serve as a deterministic jitter controller.

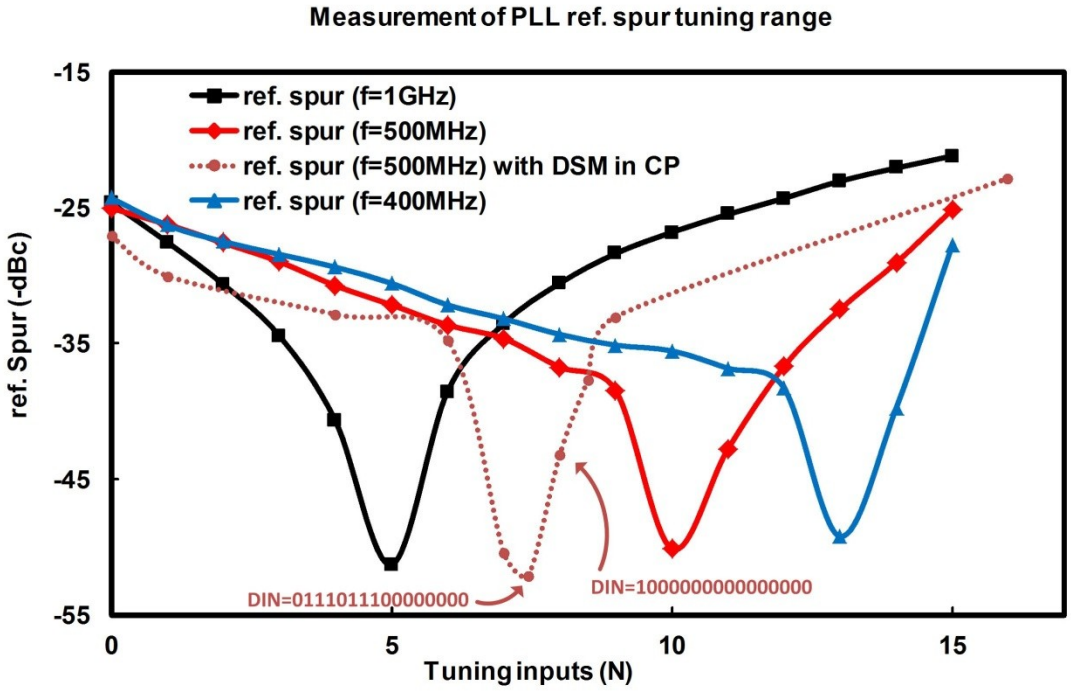


Figure 5.7. The ranges of reference spur when programming the CP current ratio with PLL output frequency of 400 MHz, 500 MHz, and 1 GHz. A fine resolution is provided by DSM on the dotted line.

Different detector transfer curves based on different output frequencies are plotted in Figure 5.8. The input to the CP ranges from 0 to 15, which varies the current level through the discharge path and therefore controls the performance of the reference spur in Figure 5.7. Off-chip calibration can be achieved since the detector output indicates the optimal reference spur. The first step is sweeping the CP inputs to modify the CP current and hence the reference spur. The second step is selecting the setting of the first 1 from the detector output. The calibration methods are easy to implement as an on-chip solution.

A further improvement can be made by sweeping the settings around the default value since the circuit should be designed to be as close as possible to its optimal performance. Few steps sweeping above and below the original setting can also acquire the best reference spur and reduce the calibration time.

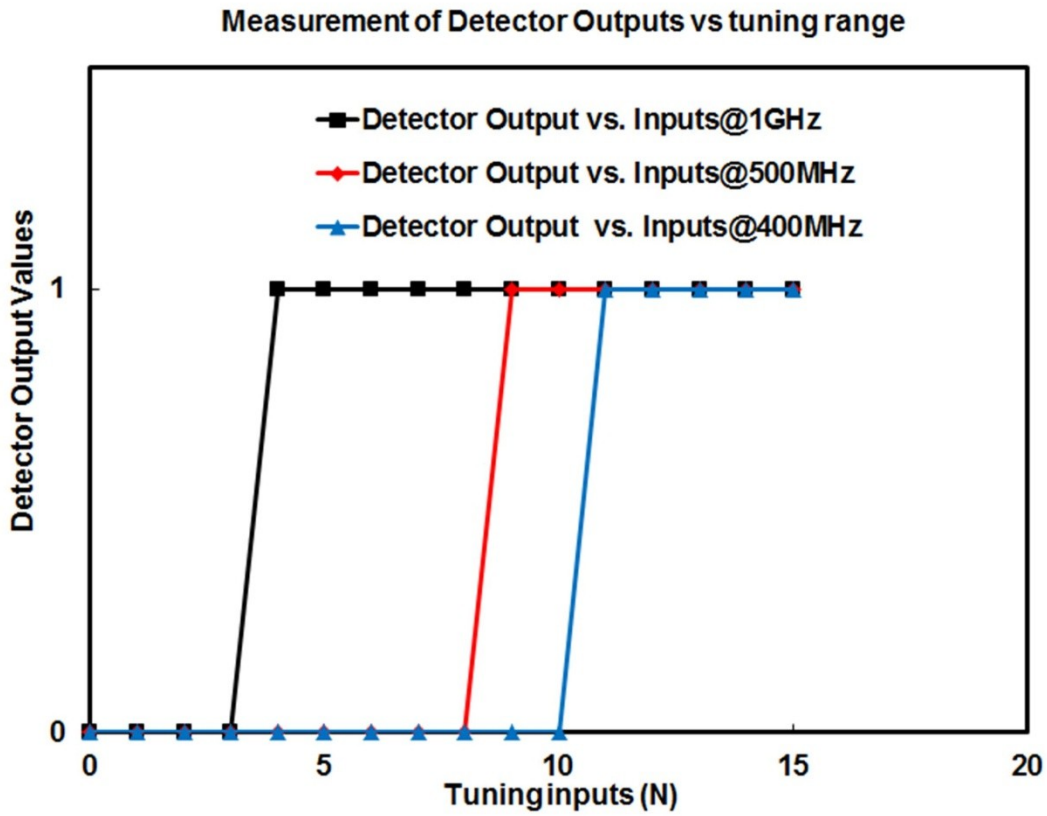


Figure 5.8. Static phase offset detector outputs is varied from zero to one when the input of CP is changed to the optimization setting.

Figure 5.9 is the calibration result of reference spur after finding the optimized value from the SPO detector output. In order to verify the method, measurements from different frequencies (400 MHz, 500 MHz, and 1 GHz) and different fabrication (TT, SS, and FF) corners are shown.

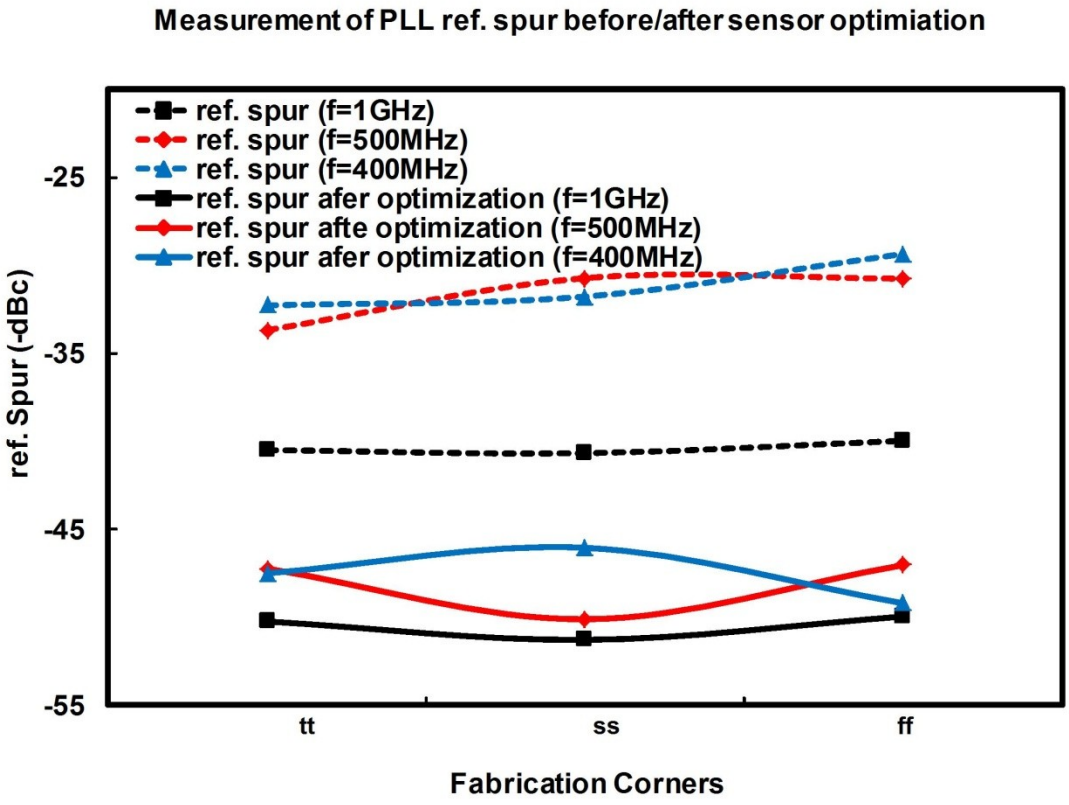


Figure 5.9. The optimized reference spurs after off-chip calibration with PLL output frequency of 400 MHz, 500 MHz, and 1 GHz.

In order to compare the performance of the PLL reference spur suppression, the figure of merit (FOM) from [52] is applied to include effects from K_{VCO}, bandwidth, reference frequency, and pole frequency. The equation is expressed as

$$FOM(dBc) = A_{Spurs}|_{dBc} - 20\log\frac{K_{VCO}}{2f_{ref}} - 20\log(\frac{f_{BW}}{f_{ref}}) - 20\log(\frac{f_p}{f_{BW}}), \qquad (30)$$

where A_{spurs} is the reference spur of the output carrier, f_{BW} is the loop bandwidth (unity-gain frequency), and f_p is the pole frequency. This equation tries to balance the impact from VCO gain and bandwidth. A small K_{VCO} would reduce the loop sensitivity to reference noise and the tuning range at the same time. On the other hand, the bandwidth limits the settling time and therefore can suppress the reference ripples. In this design, a

ring oscillator is utilized with a gain of 2.8GHz/V. The bandwidth is 220 kHz. The phase margin is more than 60 degrees for all frequency outputs. A summary of the PLL performance is listed in Table 5.1. A comparison calculating the FOM and other work are also included. The chip and hardware setup is shown in Figure 5.10.

Table 5.1. Summary and comparison of PLL performances.

Ref. / Spec.	This Work	[53]	[52]	[54]		[55]	[56]
Technology	65nm CMOS	0.18um CMOS	90nm CMOS	0.13um CMOS		0.18um CMOS	0.18um CMOS
Output Frequency (GHz)	0.4 - 1.0	2.21	3.6	0.8	2.4	2.4	5.2
Reference Frequency (MHz)	6.25	55.25	6	100	300	12	10
Reference Spur (dBc)	-53	-86	-74	-68.5	-48.3	-70.45	-68.5
f_{BW} / f_{ref}	1/28	1/20	1/20	1/10	1/30	1/12	1/50
K_{vco} / f_{ref}	800	0.9	16.67	5	3.33	5	30
Power Consumption (mW)	0.92 - 2.31	3.8	1.5	-	23	48.78	19
In-band Phase Noise (dBc/Hz)	-82.78@ 100kHz	-121@ 100kHz	-60.5@ 100kHz	-120@ 100kHz		-103@ 100kHz	-76@ 20kHz
Area (mm^2)	0.079	0.2	0.063	0.07		4.8	0.64
FOM (dBc)	-87.4	-65.09	-78.46	-68.46	-35.19	-68.83	-70.04

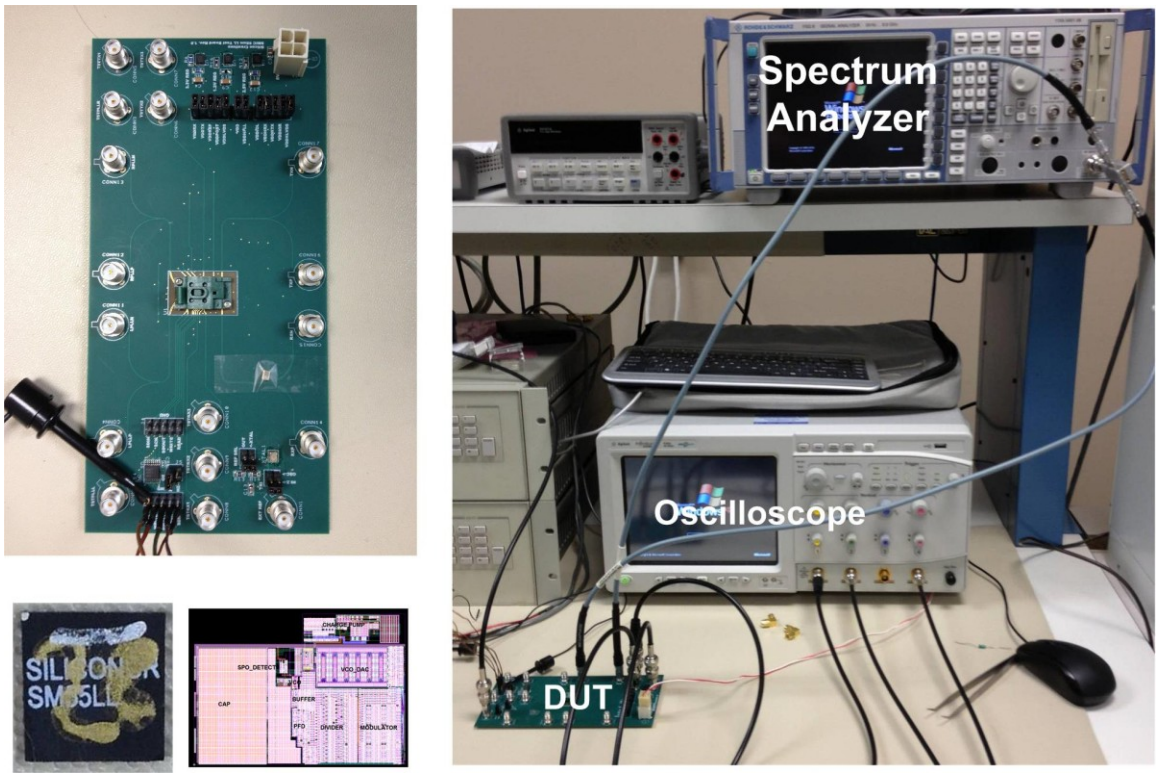


Figure 5.10. The chip and hardware measurement of the PLL with calibration circuits for reference spur suppression.

5.4 Summary

This chapter presents a PLL with an on-chip calibration circuit for reference spur suppression. The calibration circuit includes a reference spur controller which trims the charge pump current ratio for different PLL output reference spur magnitudes. A sensor for static phase offset detection is also utilized to indicate the best calibrated level. The best measured improvement in reference spur was 22.99 dB and the minimum improvement was 12 dB. Difference PLL output frequencies and different chips were tested to validate the method. The results indicate the calibration was effective by selecting the setting of the first logic high from the detector output. With implementation of a simple selection algorithm, an on-chip solution for self-calibration is possible.

CHAPTER 6: CONCLUSIONS

The final chapter concludes the research in developing analog-based sensor testing and calibration circuits for frequency synthesizer. Technique contributions of this research work are summarized in Section 6.1. Potential improvement and future directions related to the work are discussed in Section 6.2.

6.1 Technical Contributions

The dissertation investigates the design of circuits for PLL testing and calibration. PLL plays the role of synthesizing a frequency source in a communication system and is the first barrier to reduce the noise and lower the BER. The self-test of PLL is hence important due to the complexity and cost involved in a testing process, especially the characterization of noise performance. A PLL is usually designed to save specification margin for front-end circuits such as PA, LNA, mixers, and high speed LVDS IO by maintaining the clock as clean as possible. However, PVT variation degrades the devices parameters and often requires additional calibration step to compensate the performance. A robust circuit design should meet the specification over different operation conditions with minimum overhead and the aid of self-test and self-calibration. In this dissertation, multi-dimensional aspects of issues for the purpose are discussed as follows:

- The design of a robust PLL is investigated for minimum overhead. A capacitance multiplier is proposed for area reduction in the loop filter. A dual-core VCO with regulators is designed for a wide frequency coverage and good PSRR on the 60GHz application. Adaptable acquisition speed is achieved by a programmable loop filter. Solid performances of PLL are validated in CMOS

65nm process through post-layout simulation to show the feasibility of circuit techniques.

- An analog integrator is designed for the PLL loop parameters testing including charge pump current, loop bandwidth, phase margin, locking time, and VCO gain. A supervised learning methodology is used to test the performances over PVT in simulations. The methodology features low cost by extracting the response from the CUT and trained the model for specification prediction. Hardware measurement of the sensor along with a PLL in PCB design is provided as well.
- The analog integrator is further used for PLL reference spur estimation by extracting the SPO information. In the steady state, periodic offset occurs in front of the charge pump and leads to reference ripples on the tuning voltage line. The static offset between charge and discharge path can be monitored by the integrator-based sensor output DC voltage difference, which determines the reference spur performance. A PLL in PCB with programmable charge pump is implemented to validate the technique and correlation.
- A BIST for SPO estimation is proposed and featuring the full-digital interface. The implementation is simple and includes only integrators, comparators, and clock counters. A linear correlation between the counter output values and SPO is achieved in simulation. RTL implementation is feasible as well due to the digital interface.
- A self-calibration circuits for PLL reference spur is proposed. The calibration circuits includes a SPO detector and a charge pump trimming. The optimal value

of reference spur is determined by the output of SPO detector. The PLL with calibration circuits is fabricated in CMOS 65nm process with minimum and maximum improvements of 12dB and 22.99dB in reference spur suppression. The best improvement reduces the integrated jitter by 10% over a 10kHz to 10MHz bandwidth. The technique is demonstrated for a PLL output frequency from 400 MHz to 1 GHz. The ring oscillator based PLL is designed with 200 KHz bandwidth and 70 degree phase margin. Measurement results from chips across different corners are provided to verify the calibration technique.

6.2 Future Work

Self-test and self-calibration are important for an efficient production flow and a robust design. The development of testing sensor and calibration circuits for PLL parameters benefits potential on-chip "self-healing" application in PLL. This research work can be extended into the following areas in the future for improvements:

- Improvements on PLL design with minimum overhead: The optimized performances of PLL with minimum overhead is achieved through area reduction, loop programmability, frequency coverage, and supply rejection. With the aid of these techniques, PLLs are able to meet the specifications in a communication system such as a mmW wireless transceiver and a high speed wireline interface. Chip fabricated can be done for the design of PLL in order to strengthen the feasibility of overhead reduction and performance optimization.
- Feasibility of the analog-sensor based testing on random jitter: The goal of analog sensor testing is to extract the response of PLL for loop parameters and reference spur. Reference spur belongs to deterministic noise and contributes to

the output long-term jitter. The challenging topic would be to extract the response for random noise. Due to its randomization and low sensitivity, it is difficult for designers to predict the performance through a sensor. An optional methodology is indirect specification estimation via extracting other highly related parameters. The gain of VCO correlates the output phase noise to a certain degree. The bandwidth identifies the cut-off frequency of the loop and conveys useful information for noise as well. This testing method can be experimented by extracting the performance of loop bandwidth and VCO gain first, and correlating the phase noise from PLL.

- Implementation of on-chip integrators: The functionality of integrator provides high correlation with PLL loop operation. One of the goals of sensor design is to implement self-test and self-calibration circuits as an on-chip solution. Since the integrator is validated in PCB design, an on-chip design with PLL can further increase the contribution. The design may suffer more trade-off for on-chip performances such as time constant optimization. A large resistor needs to be used for a better area utilization.
- Improvements on PLL reference spur calibration: The design of reference spur suppression circuits effectively improves the spur performance by SPO detection. In order to achieve a "self-healing" system, a combination of the two circuits for self-test and self-calibration is a further fulfillment. A charge pump design with more current trimming bits increases the resolution for spur suppression as well. In addition, the function of SPO detection can be verified if the UP and DN signals are connected to external interface for phase comparison. The offset in

SPO detection can be therefore found and used to increase the resolution of calibration.

REFERENCES

[1] USB Implementers Forum, "Universal Serial Bus 3.0 Specification," June 2011 [Online]. Available: http://www.usb.org/developers/docs/usb_30_spec_071012.zip (Accessed Aug. 12, 2012).

[2] High-Definition Multimedia Interface, "What functionality was added to each version of HDMI?" [Online]. Available: http://www.hdmi.org/learningcenter/faq.aspx#12 (Accessed Aug. 12, 2012).

[3] VESA, "Why DisplayPort." [Online]. Available: http://www.vesa.org/displayport-developer/why-displayport (Accessed Aug. 12, 2012).

[4] Intel, "Thunderbolt™ Technology: Overview." [Online]. Available: http://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/thunderbolt-overview-brief.pdf (Accessed Aug. 12, 2012).

[5] Status of Project IEEE 802.11ac [Online]. Available: http://www.ieee802.org/11/Reports/tgac_update.htm (Accessed Aug. 12, 2012).

[6] Wireless Gigabit Alliance, "WiGig White Paper: Defining the Future of Multi-Gigabit Wireless Communications," July 2010 [Online]. Available: http://wirelessgigabitalliance.org/?getfile=1510 (Accessed Aug. 12, 2012).

[7] Status of Project IEEE 802.11ad [Online]. Available: http://www.ieee802.org/11/Reports/tgad_update.htm (Accessed Aug. 12, 2012).

[8] WirelessHD, "WirelessHD Specification Version 1.1 Overview," May 2010. [Online]. Available: http://www.wirelesshd.org/pdfs/WirelessHD-Specification-Overview-v1.1May2010.pdf (Accessed Aug. 12, 2012).

[9] M. Toner & G. Roberts, “A BIST scheme for an SNR test of a sigma-delta ADC”, Proceedings of ITC, 1993.

[10] V.D. Agrawal, C.R. Kime, and K.K. Saluja, “A Tutorial on Built-In Self-Test, Part 1: Principles,” IEEE Design and Test of Computers, pp. 73-82, Mar. 1993.

[11] V.D. Agrawal, C.R. Kime, and K.K. Saluja, “A Tutorial on Built-In Self-Test, Part 2: Applications,” IEEE Design and Test of Computers, pp. 69-77, Jun. 1993.

[12] T.-H. Lin and W. J. Kaiser, “A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop,” IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 424–431, Mar. 2001.

[13] D. Banerjee, PLL Performance, Simulation, and Design, 4th ed. Santa Clara, CA: National Semiconductor, 2005.

[14] J. Laskar, S. Chakraborty, M. Tentzeris, F. Bien, A.-V Pham, Wireless Communication System Architectures, in Advanced Integrated Communication Microsystems, 1st. ed. Hoboken, NJ: John Wiley & Sons, 2008, ch. 2.

[15] Mike Harwood, et al., “A 12.5Gb/s SerDes in 65nm CMOS Using a Baud Rate ADC with Digital Receiver Equalization and Clock Recovery,” ISSCC Dig. Tech. Papers, pp. 68-69, Feb., 2007.

[16] B. Razavi, RF Microelectronics. Englewood Cliffs, NJ: Prentice-Hall, 1998, ch. 8.

[17] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching properties of MOS transistors,” IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[18] FRIEDMAN, Jerome H. Multivariate adaptive regression splines. The annals of statistics, 1-67, 1991.

[19] S. S. Akbay and A. Chatterjee, “Built-in test of RF components using mapped feature extraction sensors,” inProc. IEEE VLSI Test Symp., 2005, pp. 243–248.

[20] R. Voorakaranam, S. Cherubal, and A. Chatterjee, “A signature test framework for rapid production testing of RF circuits,” in Proc. Des., Autom. Test Eur., 2002, pp. 186–191.

[21] T. Lin et al., “An agile VCO frequency calibration technique for a 10-GHz CMOS PLL,” IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 340–349, Feb. 2007.

[22] B. Razavi, A 60-GHz direct-conversion CMOS receiver, IEEE ISSCC Dig. Tech. Papers, Feb. 2005, pp. 400–401.

[23] C.-S. Choi, E. Grass, F. Herzel, M. Piz, et al., “60-GHz OFDM hardware demonstrators in SiGe BiCMOS: state-of-the-art and future development,” IEEE PIMRC 2008, Cannes, France, Sep. 2008.

[24] C. Marcu, D. Chowdhury, C. Thakkar, L. Kong, M. Tabesh, J. Park, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, A. M. Niknejad, and E. Alon, “A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry,” IEEE ISSCC Dig. Tech. Papers, Feb. 2009.

[25] A. Lacatia, S. Levantino, and C. Samori, Integrated Frequency Synthesizers for Systems, 1st ed. Cambridge, UK: Cambridge Univ. Press, 2007.

[26] K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, S.H.K. Embabi, “A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier,” IEEE J. Solid-State Circuits, vol.38, no.6, pp. 866- 874, June 2003.

[27] D. Miyashita et al., “A −104dBc/Hz in-band phase noise 3GHz all digital PLL with phase interpolation based hierarchical time to digital convertor,” Symposium on VLSI Circuits (VLSIC), pp.112,113, June 2011.

[28] H. Hedayati and B. Bakkaloglu, “A 3 GHz wideband sigma-delta fractional-N synthesizer with voltage-mode exponential CP-PFD,” in IEEE Radio Frequency Integrated Circuits Symposium, pp. 325–328, Jun. 2009.

[29] Y. Sun et al., “Low-noise fractional-n PLL design with mixed-mode triple-input LC VCO in 65 nm CMOS,” in Proc. IEEE Radio Frequency Integrated Circuits Symposium, pp. 61–64, May 2010.

[30] D. Park and S. Cho, “A 14.2mW 2.55-to-3GHz cascaded PLL with reference injection, 800MHz delta-sigma modulator and 255fsrms integrated jitter in 0.13μm CMOS”, ISSCC Dig. Tech. Papers, pp. 344-346, Feb. 2012.

[31] B.A. Floyd, “A 16-18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers”, IEEE JSSC, vol. 43, no. 5, pp. 1076 –1086, May 2008.

[32] O. Richard, A. Siligaris, F. Badets, C. Dehos, C. Dufis, P. Busson, P. Vincent, D. Belot, and P. Urard, “A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for wireless HD applications”, ISSCC Dig. Tech. Papers, pp. 252 –253, Feb. 2010.

[33] J. Osorio et al., “A 21.7-to-27.8GHz 2.6-degrees-rms 40mW frequency synthesizer in 45nm CMOS for mm-wave communication applications,” ISSCC Dig. Tech. Papers, pp. 278-280, Feb. 2011.

[34] B. Sadhu et al., "A 21.8-27.5GHz PLL in 32nm SOI using Gm linearization to achieve -130dBc/Hz phase noise at 10MHz offset from a 22GHz carrier," IEEE Radio Frequency Integrated Circuits Symposium, pp. 75-78, June 2012.

[35] S. Sunter and A. Roy, "BIST for phase-locked loops in digital applications," in Proc. Int. Test Conf., 1999, pp. 532–540.

[36] A. Aktas and M. Ismail, "CMOS PLL calibration techniques," IEEE Circuits Devices Mag., vol. 20, no. 5, pp. 6–11, Sept./Oct. 2004.

[37] C. Thambidurai and N. Krishnapura, "On Pulse Position Modulation and Its Application to PLLs for Spur Reduction," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 58, no. 7, pp. 1483-1496 2011.

[38] F. Barale; G.B. Iyer; B.G. Perumana; P. Sen; S. Sarkar; A. Rachamadugu; N. Dudebout; S. Pinel; J. Laskar, "Pulse shaping and clock data recovery for multi-gigabit standard compliant 60 GHz digital radio," IEEE International Microwave Symposium (IMS), pp.908-911, 23-28 May 2010.

[39] L.-C. Hwang, "Area-efficient and self-biased capacitor multiplier for on-chip loop filter," Electronics Letters , vol.42, no.24, pp.1392-1393, Nov. 2006.

[40] Liu, L.C. and Li, B.H. , "Fast locking scheme for PLL frequency synthesizer," Electronics Letters , vol.40, no.15, pp. 918- 920, Jul. 2004.

[41] N. Tzou, D. Bhatta, S.-W. Hsiao, H.W. Choi, A. Chatterjee, "Low-Cost Wideband Periodic Signal Reconstruction Using Incoherent Undersampling and Back-end Cost Optimization," IEEE International Test Conference (ITC), pp. 1-10, Nov. 2012.

[42] P.N. Variyam, S. Cherubal and A. Chatterjee, “Prediction of analog performance parameters using fast transient testing”, IEEE Transactions on CAD of integrated circuits and systems, pp. 349-361, Mar. 2002.

[43] P.N. Variyam and A. Chatterjee, “Enhancing test effectiveness for analog circuits using synthesized measurements”, Proc. VLSI Test Symp. , pp. 132-137, Apr. 1998.

[44] B. R. Veillette and G. W. Roberts, “On-chip measurement of the jitter transfer function of charge pump phase-locked loops,” in Proc. IEEE Int. Test Conf., Washington, DC, Nov. 1997, pp. 776–785.

[45] J. Kim, “On-chip measurement of jitter transfer and supply sensitivity of PLL/DLLs,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 6, pp. 449–453, Jun. 2009.

[46] S. Sunter and A. Roy, “Purely digital BIST for any PLL or DLL,” in Proc. Euro. Test Symp., 2007, pp. 185–192.

[47] J. S. Lee et al., “Charge pump with perfect current matching characteristics in phase-locked loops,” Electron. Lett., vol. 36, no. 23, pp. 1907–1908, Nov. 2000.

[48] W. Rhee, “Design of high-performance CMOS charge pumps in phase locked loops,” in Proc. IEEE Int. Symp. Circuits and Systems, 1999, pp. 545–548.

[49] S.-W. Hsiao, N. Tzou, and A. Chatterjee, “A Programmable BIST Design for PLL Static Phase Offset Estimation and Clock Duty Cycle Detection,” in Proc. VLSI Test Symposium (VTS), pp. 1-6, Apr. 2013.

[50] S.-W. Hsiao, C.-C. Chen, R. Caplan, J. Galloway, B. Gray, and A. Chatterjee, “Phase-Locked Loop Design with SPO Detection and Charge Pump Trimming for

Reference Spur Suppression," submitted in Proc. VLSI Test Symposium (VTS), Apr. 2014.

[51] B. Gray, M. Masood, J. Galloway, R. Caplan, and J.S. Kenney, "Microdegree frequency and phase difference control using fractional-N PLL synthesizers," IEEE International Microwave Symposium (IMS), pp.1-3, June 2012.

[52] M.M. Elsayed, et al., "A Spur-Frequency-Boosting PLL With a -74 dBc -Spur Suppression in 90 nm Digital CMOS," IEEE J. Solid-State Circuits, vol. PP, no.99, pp.1-14, Jul. 2013.

[53] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "Spur-reduction techniques for PLLs using sub-sampling phase detection," IEEE Int. Solid-State Circuits Conf. (ISSCC), pp. 474–475, Feb. 2010.

[54] Z. Cao, Y. Li, and S. Yan, "A0.4 ps-RMS-jitter 1–3 GHz ring-oscillator PLL using phase-noise preamplification," IEEE J. Solid-State Circuits, vol. 43, no. 9, pp. 2079–2089, Sep. 2008.

[55] K. J.Wang, A. Swaminathan, and I.Galton, "Spurious tone suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL," in IEEE ISSCC Dig. Tech. Papers, 2008, pp. 342–343.

[56] C.-F. Liang, S.-H. Chen, and S.-I. Liu, "A digital calibration technique for charge pumps in phase-locked systems," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 390–398, Feb. 2008.

PUBLICATIONS

[1] **S.-W. Hsiao**, S.-C.Shin, and M.C.-H. Leung, "Embedded baseband IQ AGC and OOK demodulator in CMOS 45nm 60GHz single-chip transceiver," in *Proc. of Asia-Pacific Microwave Conference (APMC)*, pp. 1542-1545, Dec. 2011.

[2] **S.-W. Hsiao** and D. Yeh, "A 1-V CMOS 65nm frequency synthesizer design with programmable acquisition speed," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1-4, Aug. 2011.

[3] **S.-W. Hsiao**, "An area-efficient 3.5GHz fractional-N frequency synthesizer with capacitor multiplier in millimeter-wave gigabit wireless communication," *IEEE Wireless and Microwave Technology Conference (WAMICON)*, pp. 1-5, Apr. 2012.

[4] **S.-W. Hsiao**, N. Tzou, D. Bhatta, and A. Chatterjee, "24GHZ Dual Core PLL Design for 60 GHz Transceiver and Efficient Validation Methodology," in *Proc. of Asia-Pacific Microwave Conference (APMC)*, Dec. 2012.

[5] **S.-W. Hsiao** and M.C.-H. Leung, "A Programmable 1-V CMOS 65nm Frequency Synthesizer Design in 60GHZ wireless transceiver," Journal of Circuits, Systems and Computers (JCSC), vol. 21, issue 6, Nov. 2012.

[6] **S.-W. Hsiao**, N. Tzou, A. Chatterjee, "A Programmable BIST Design for PLL Static Phase Offset Estimation and Clock Duty Cycle Detection," in *Proc. VLSI Test Symposium (VTS)*, pp. 1-6, Apr. 2013.

[7] **S.-W. Hsiao**, X. Wang, A. Chatterjee, "Analog Sensor Based Testing of Phase-Locked Loop Dynamic Performance Parameters," accepted in *Asian Test Symposium (ATS)*, Nov. 2013.

[8] **S.-W. Hsiao**, C.-C. Chen, R. Caplan, J. Galloway, B. Gray, and A. Chatterjee, "Phase-Locked Loop Design with SPO Detection and Charge Pump Trimming for Reference Spur Suppression," accepted by *Proc. VLSI Test Symposium (VTS)*, Apr. 2014.

[9] J. Laskar, S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Dawn, M. Leung, F. Barale, D. Yeh, S.-C. Shin, **S.-W. Hsiao**, K. Chuang, E. Juntunen, G. Iyer, A. Muppalla, P. Melet, "On the development of CMOS mmW and sub-THz phased array technology

for communication/sensing nodes," IEEE MTT-S international Microwave Symposium Digest, pp. 1312-1315, May 2010.

[10] S.-C.Shin, **S.-W. Hsiao**, J.C.-H. Poh, and J. Laskar, "A systematic measurement technique to characterize bimodal oscillation for CMOS Quadrature LC-VCO," in *Proc. of Asia-Pacific Microwave Conference (APMC)*, pp. 1051-1054, Dec. 2010.

[11] S.-C.Shin, C. Liu, S.-H. Fan, Y.-T. Hsueh, **S.-W. Hsiao**, and G.-K. Chang, "A versatile 60 GHz CMOS phased-array transmitter chipset for broadband radio-over-fiber systems," in *Proc. of Asia-Pacific Microwave Conference (APMC)*, pp. 1718-1721, Dec. 2011.

[12] S.-C.Shin, and M.C.-H. Leung, **S.-W. Hsiao**, "A temperature variation compensated 60-GHz low-noise amplifier in 90-nm CMOS technology," in *Proc. of Asia-Pacific Microwave Conference (APMC)*, pp. 211-214, Dec. 2011.

[13] N. Tzou, D. Bhatta, **S.-W. Hsiao**, H.W. Choi, A. Chatterjee, "Low-Cost Wideband Periodic Signal Reconstruction Using Incoherent Undersampling and Back-end Cost Optimization," *IEEE International Test Conference (ITC)*, pp. 1-10, Nov. 2012.

[14] **S.-W. Hsiao**, Y.-C. Huang, D. Liang, H.-W. K. Chen, and H.-S. Chen, "A 1.5-V 10-ppm//spl deg/C 2nd-order curvature-compensated CMOS bandgap reference with trimming," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 565-568, May 2006.

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